

**N- AND P-Channel Logic Level Enhancement Mode MOSFET**

# MTC2402Q8

	N-CH	P-CH
$BV_{DSS}$	20V	-20V
$I_{D@ TA=25\text{ }^{\circ}\text{C}}$	8.5A	-7.9A
$R_{DSON}(typ.) @V_{GS}=(-)4.5V$	15.5m $\Omega$	20.3m $\Omega$
$R_{DSON}(typ.) @V_{GS}=(-)2.5V$	19.5m $\Omega$	25.0m $\Omega$

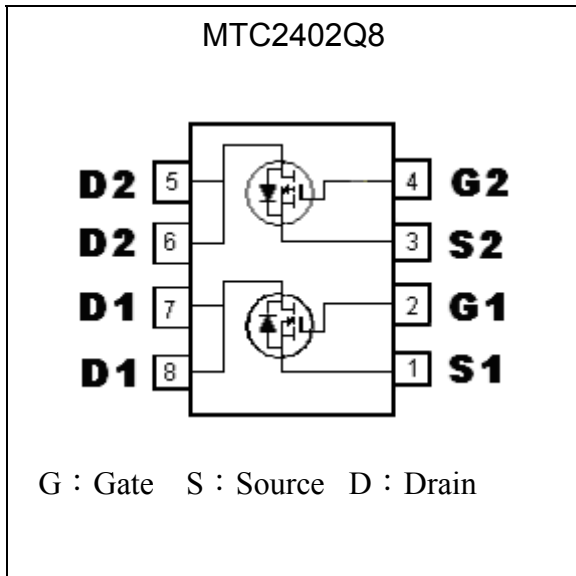
**Description**

The MTC2402Q8 consists of a N-channel and a P-channel enhancement-mode MOSFET in a single SOP-8 package, providing the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness. The SOP-8 package is universally preferred for all commercial-industrial surface mount applications.

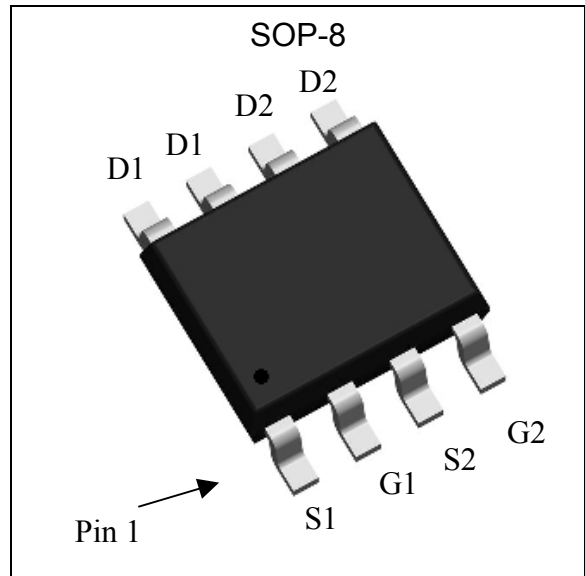
**Features**

- Simple drive requirement
- Low on-resistance
- Fast switching speed
- Pb-free lead plating and halogen-free package

**Equivalent Circuit**

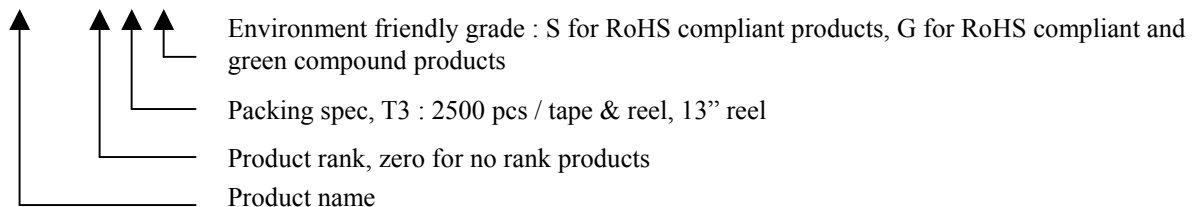


**Outline**



**Ordering Information**

Device	Package	Shipping
MTC2402Q8-0-T3-G	SOP-8 (Pb-free lead plating and halogen-free package)	2500 pcs / tape & reel





**Absolute Maximum Ratings** (T<sub>C</sub>=25°C, unless otherwise noted)

Parameter	Symbol	Limits		Unit	
		N-channel	P-channel		
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	20	-20	V	
Gate-Source Voltage	V <sub>GS</sub>	±12	±12	V	
Continuous Drain Current (Note 2)	I <sub>D</sub>	T <sub>A</sub> =25 °C, V <sub>GS</sub> =4.5V (-4.5V)	8.5	-7.9	A
		T <sub>A</sub> =70 °C, V <sub>GS</sub> =4.5V (-4.5V)	6.8	-6.3	
Pulsed Drain Current (Note 1)	I <sub>DM</sub>	40	-30	A	
Power Dissipation (Note 2)	P <sub>D</sub>	T <sub>A</sub> =25°C	2.5		W
		T <sub>A</sub> =70°C	1.6		
Operating Junction and Storage Temperature Range	T <sub>j</sub> ; T <sub>stg</sub>	-55~+150		°C	

**Thermal Data**

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	R <sub>θJC</sub>	25	°C/W
Thermal Resistance, Junction-to-ambient, max	R <sub>θJA</sub>	50 (Note 2)	
Lead Temperature(1/16" from case, for 10 seconds)	T <sub>L</sub>	275	°C

Note : 1.Pulse width limited by maximum junction temperature.  
 2.Surface mounted on 1 in<sup>2</sup> copper pad of FR-4 board, pulse width≤10s.

**N-Channel Electrical Characteristics** (T<sub>C</sub>=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
<b>Static</b>					
BV <sub>DSS</sub>	20	-	-	V	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA
V <sub>GS(th)</sub>	0.5	-	1.2		V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA
I <sub>GSS</sub>	-	-	±100	nA	V <sub>GS</sub> =±12V, V <sub>DS</sub> =0V
I <sub>DSS</sub>	-	-	1	μA	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V
	-	-	25		V <sub>DS</sub> =20V, V <sub>GS</sub> =0V, T <sub>j</sub> =125°C
*R <sub>DS(ON)</sub>	-	15.5	22	mΩ	V <sub>GS</sub> =4.5V, I <sub>D</sub> =8A
	-	19.5	32		V <sub>GS</sub> =2.5V, I <sub>D</sub> =5.2A
*G <sub>FS</sub>	-	11.3	-	S	V <sub>DS</sub> =5V, I <sub>D</sub> =3A
<b>Dynamic</b>					
C <sub>iss</sub>	-	717	995	pF	V <sub>DS</sub> =10V, V <sub>GS</sub> =0V, f=1MHz
C <sub>oss</sub>	-	100	96		
C <sub>rss</sub>	-	94	115		
*t <sub>d(ON)</sub>	-	7.8	16	ns	V <sub>DS</sub> =10V, I <sub>D</sub> =1A, V <sub>GS</sub> =4.5V, R <sub>G</sub> =10Ω
*t <sub>r</sub>	-	19	38		
*t <sub>d(OFF)</sub>	-	47.8	96		
*t <sub>f</sub>	-	18.8	38		
*Q <sub>g</sub>	-	8	11	nC	V <sub>DS</sub> =10V, I <sub>D</sub> =5A, V <sub>GS</sub> =4.5V
*Q <sub>gs</sub>	-	1.2	1.6		
*Q <sub>gd</sub>	-	2.8	3.6		



Body Diode					
*I <sub>S</sub>	-	-	1.9	A	V <sub>GS</sub> =0V, I <sub>S</sub> =1A  I <sub>F</sub> =1A, dI <sub>F</sub> /dt=100A/μs
*I <sub>SM</sub>	-	-	7.6		
*V <sub>SD</sub>	-	0.77	1.2	V	
*t <sub>rr</sub>	-	7.9	-	ns	
*Q <sub>rr</sub>	-	2.8	-	nC	

\*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

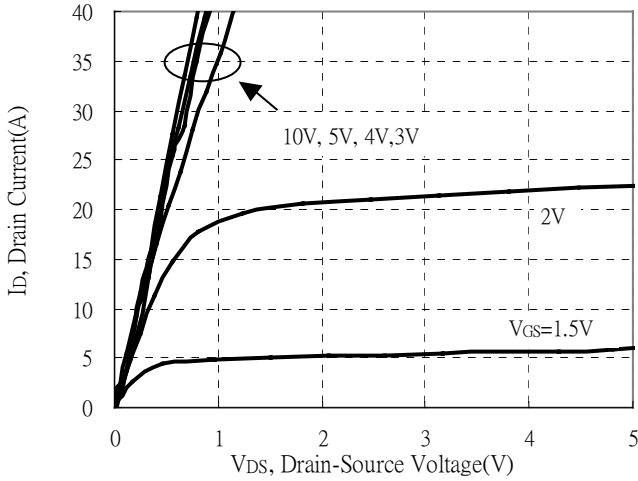
**P-Channel Electrical Characteristics (T<sub>c</sub>=25°C, unless otherwise specified)**

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
<b>Static</b>					
BV <sub>DSS</sub>	-20	-	-	V	V <sub>GS</sub> =0V, I <sub>D</sub> =-250μA
V <sub>GS(th)</sub>	-0.5	-	-1.2		V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA
I <sub>GSS</sub>	-	-	±100	nA	V <sub>GS</sub> =±12V, V <sub>DS</sub> =0V
I <sub>DSS</sub>	-	-	-1	μA	V <sub>DS</sub> =-20V, V <sub>GS</sub> =0V
	-	-	-25		V <sub>DS</sub> =-20V, V <sub>GS</sub> =0V, T <sub>j</sub> =125°C
*R <sub>DSON</sub>	-	20.3	28	mΩ	V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-5A
	-	25.0	36		V <sub>GS</sub> =-2.5V, I <sub>D</sub> =-4A
*G <sub>FS</sub>	-	17.2	-	S	V <sub>DS</sub> =-5V, I <sub>D</sub> =-3A
<b>Dynamic</b>					
C <sub>iss</sub>	-	2254	2930	pF	V <sub>DS</sub> =-10V, V <sub>GS</sub> =0V, f=1MHz
C <sub>oss</sub>	-	176	229		
C <sub>rss</sub>	-	133	175		
*t <sub>d(ON)</sub>	-	14.6	29	ns	V <sub>DS</sub> =-10V, I <sub>D</sub> =-1A, V <sub>GS</sub> =-4.5V, R <sub>G</sub> =10Ω
*t <sub>r</sub>	-	24.4	50		
*t <sub>d(OFF)</sub>	-	223.2	446		
*t <sub>f</sub>	-	109	218		
*Q <sub>g</sub>	-	22.9	30	nC	V <sub>DS</sub> =-10V, I <sub>D</sub> =-5A, V <sub>GS</sub> =-4.5V
*Q <sub>gs</sub>	-	3.2	4.2		
*Q <sub>gd</sub>	-	4.7	6.1		
<b>Body Diode</b>					
*I <sub>S</sub>	-	-	-1.9	A	V <sub>GS</sub> =0V, I <sub>S</sub> =-6.8A  I <sub>F</sub> =-6.8A, dI <sub>F</sub> /dt=100A/μs
*I <sub>SM</sub>	-	-	-7.6		
*V <sub>SD</sub>	-	-0.88	-1.2	V	
*t <sub>rr</sub>	-	9.8	-	ns	
*Q <sub>rr</sub>	-	4.2	-	nC	

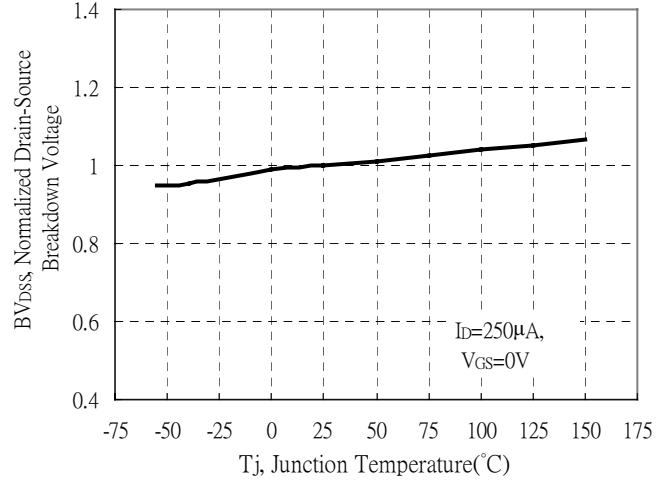
\*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

**Typical Characteristics : Q1( N-channel )**

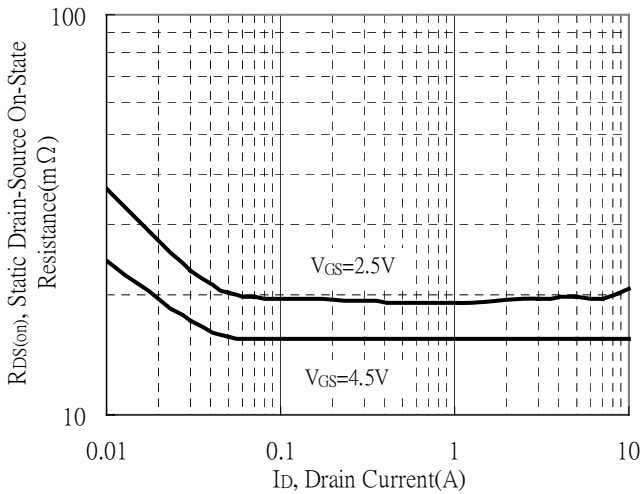
Typical Output Characteristics



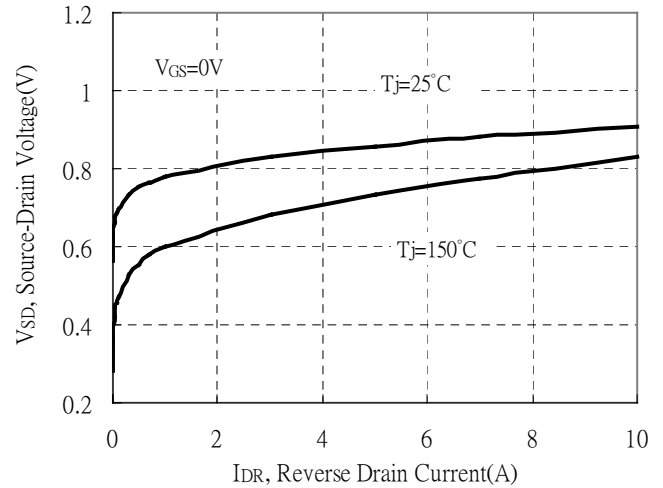
Brekdown Voltage vs Ambient Temperature



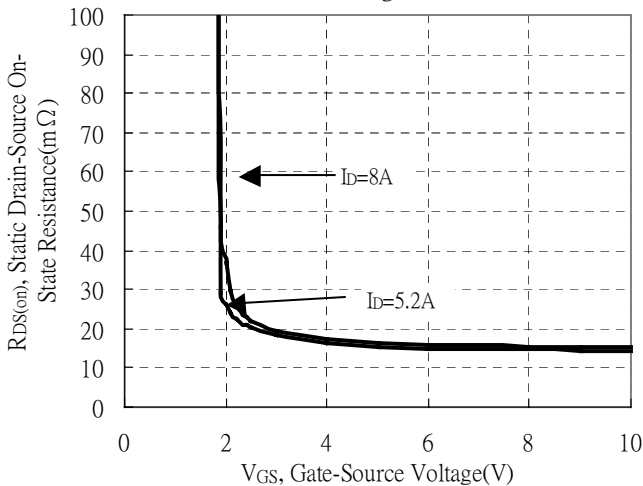
Static Drain-Source On-State resistance vs Drain Current



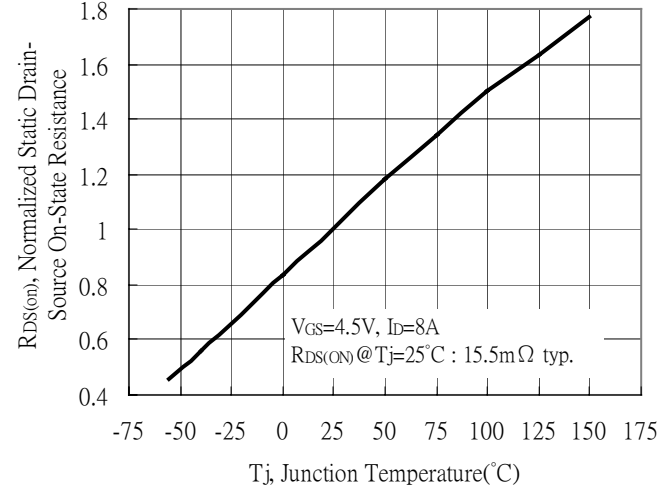
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

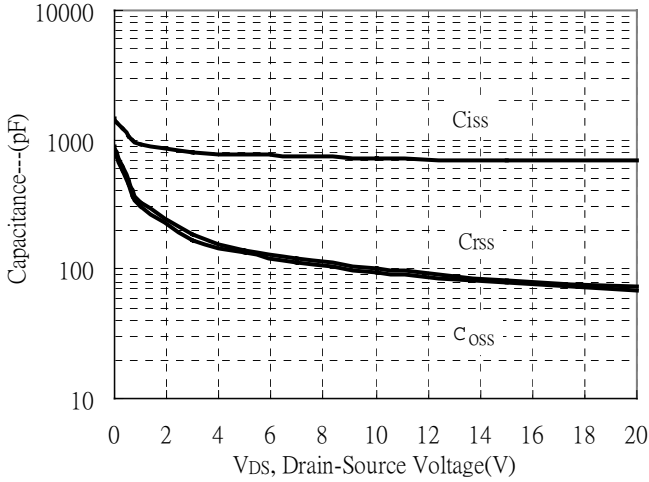


Drain-Source On-State Resistance vs Junction Temperature

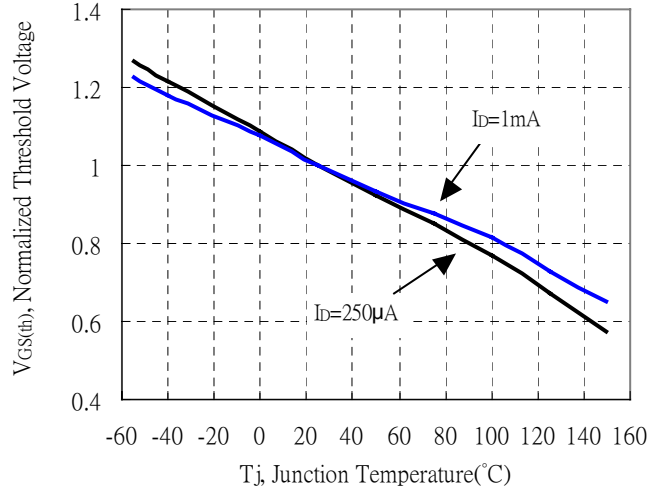


**Typical Characteristics(Cont.) : Q1( N-channel)**

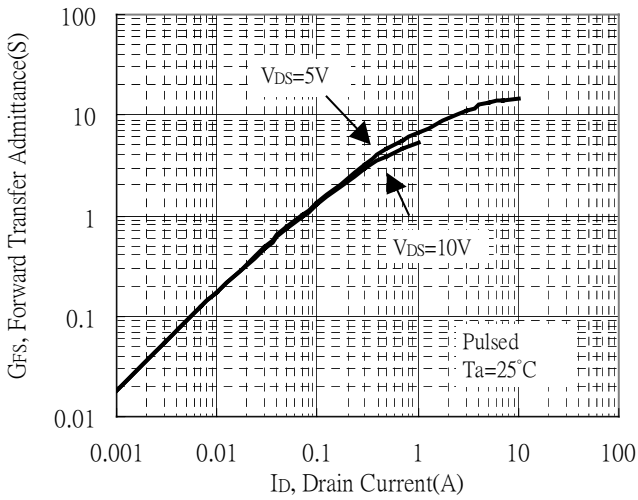
Capacitance vs Drain-to-Source Voltage



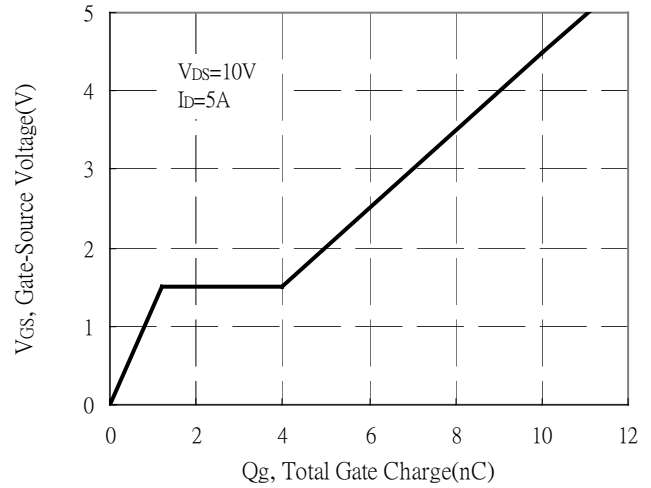
Threshold Voltage vs Junction Temperature



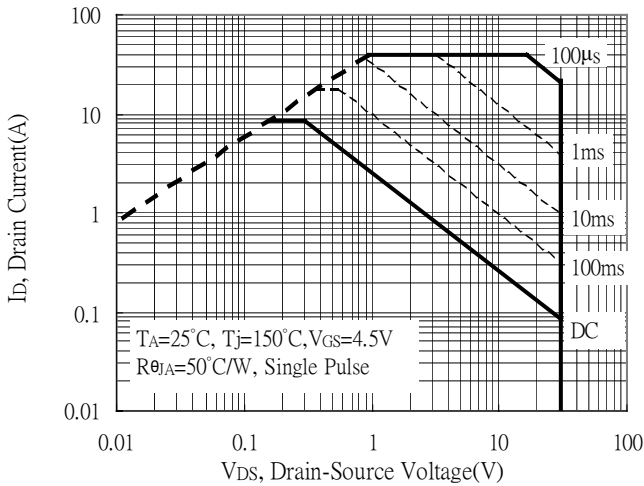
Forward Transfer Admittance vs Drain Current



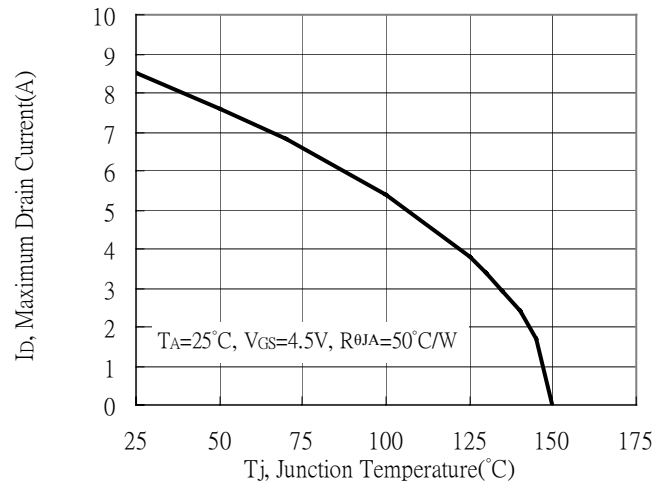
Gate Charge Characteristics



Maximum Safe Operating Area

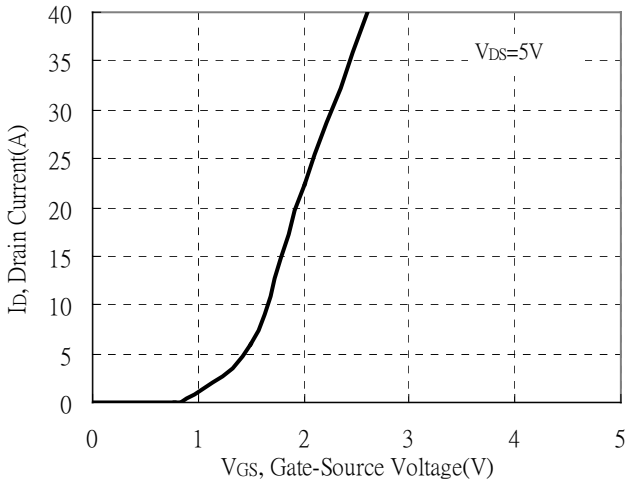


Maximum Drain Current vs Junction Temperature

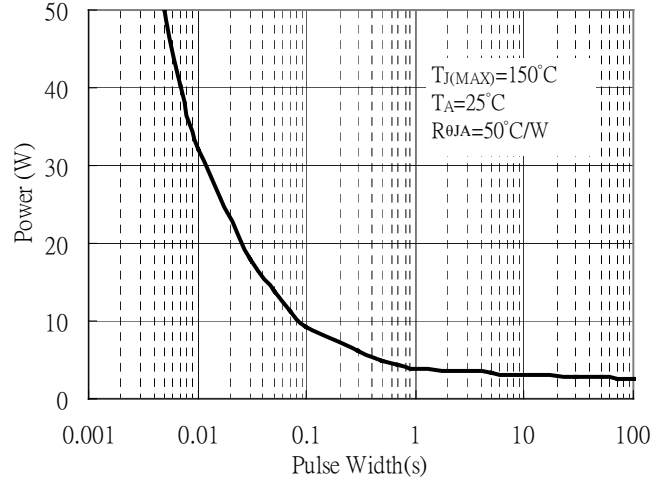


**Typical Characteristics(Cont.) : Q1( N-channel)**

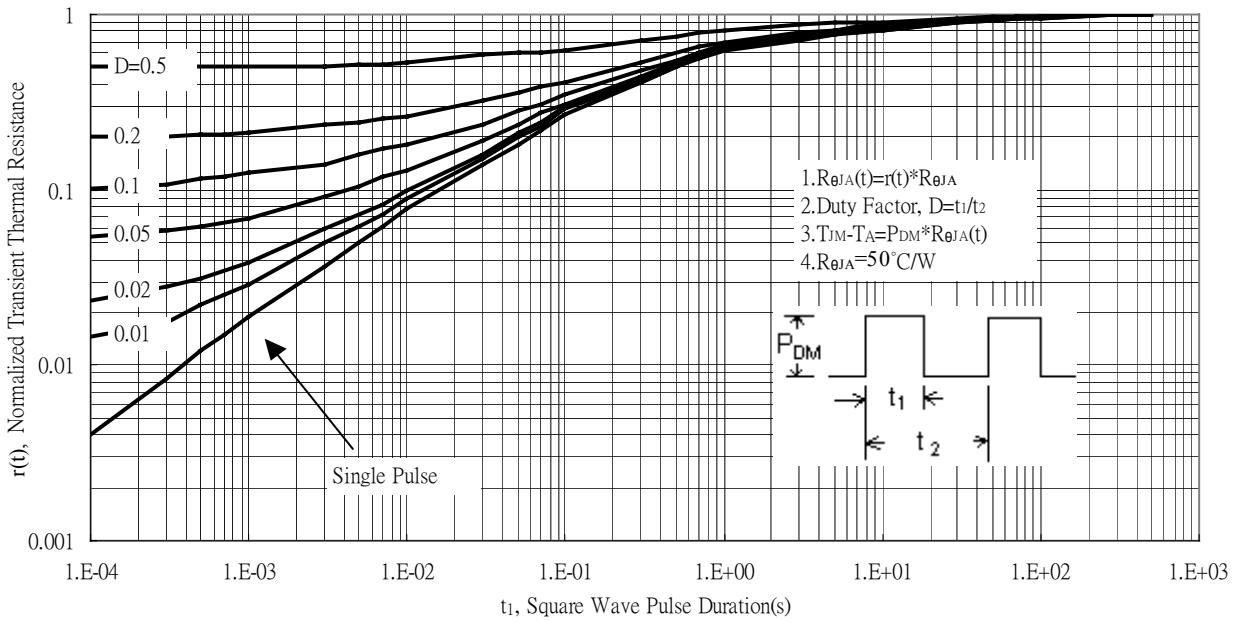
Typical Transfer Characteristics



Single Pulse Power Rating, Junction to Ambient  
 (Note on page 2)

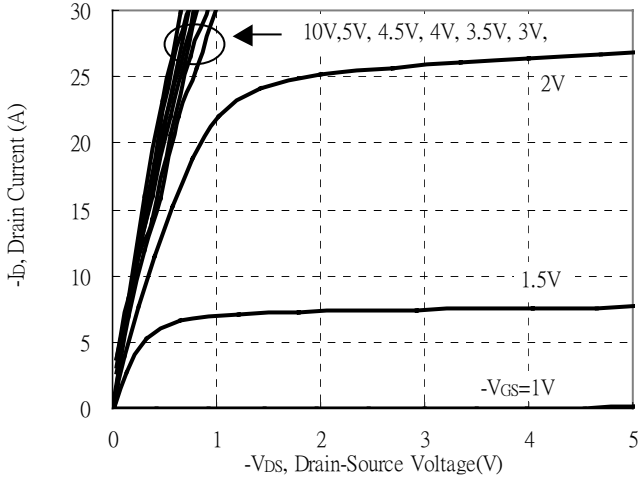


Transient Thermal Response Curves

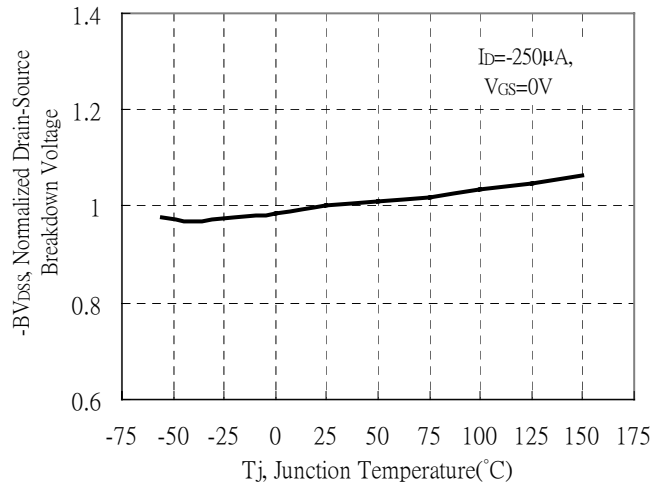


**Typical Characteristics : Q2( P-channel)**

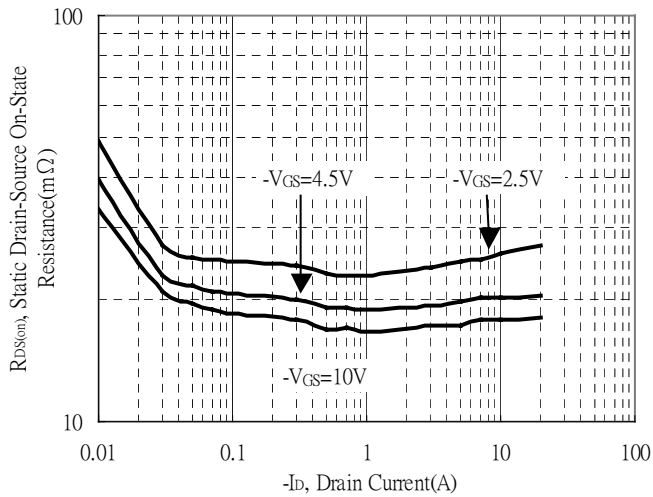
Typical Output Characteristics



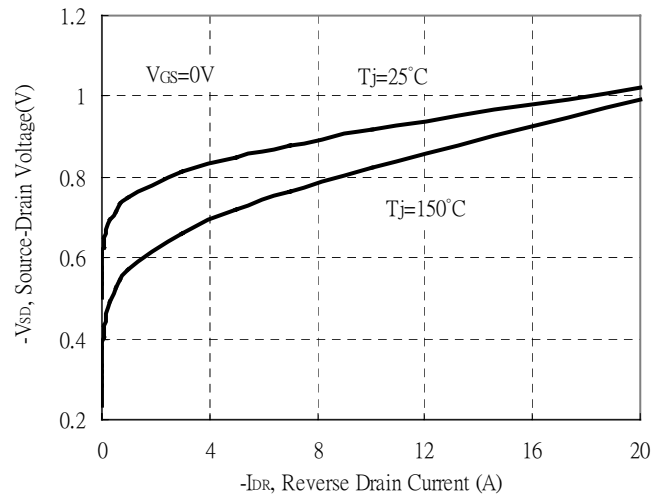
Breakdown Voltage vs Ambient Temperature



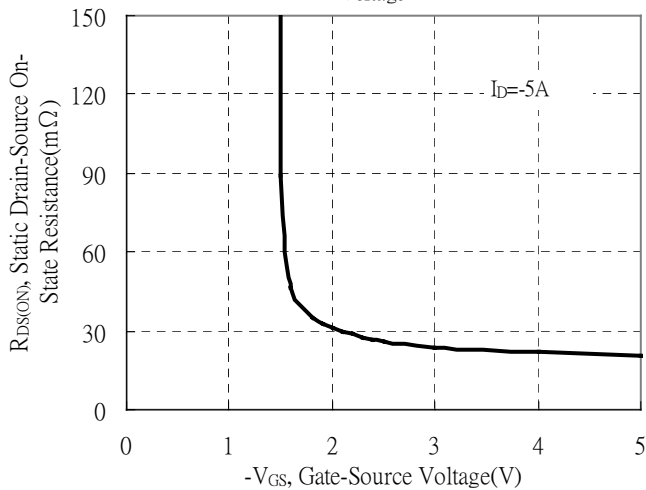
Static Drain-Source On-State resistance vs Drain Current



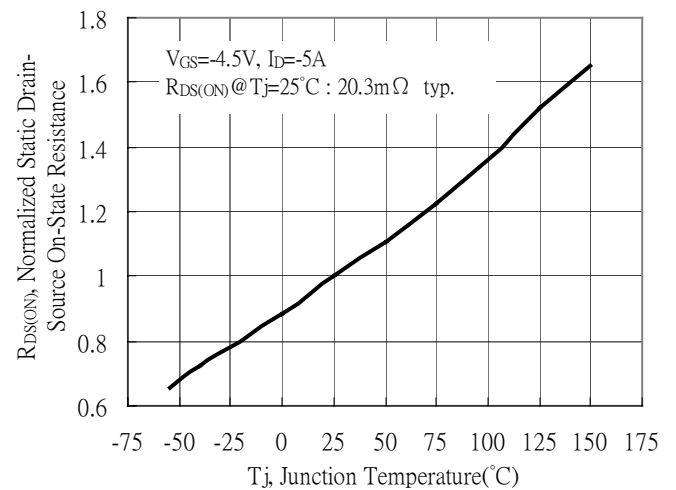
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

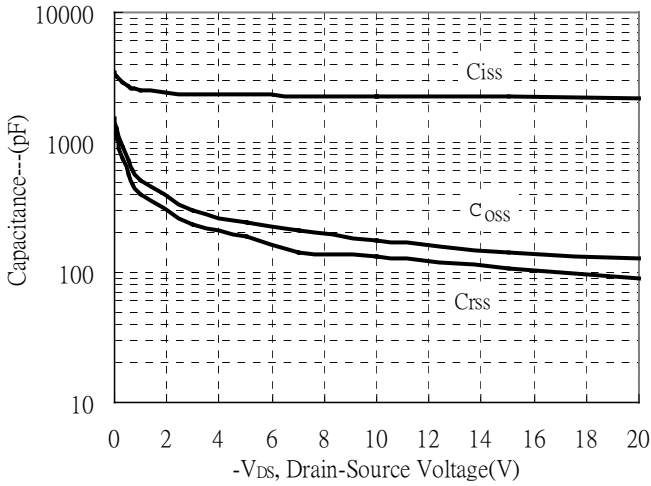


Drain-Source On-State Resistance vs Junction Temperature

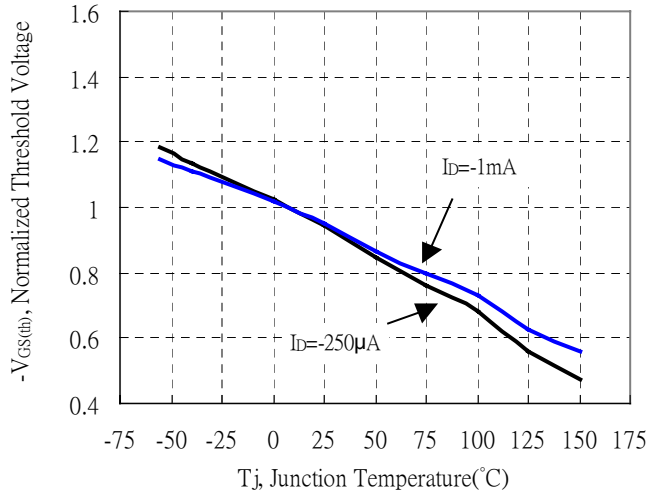


**Typical Characteristics(Cont.) : Q2(P-channel)**

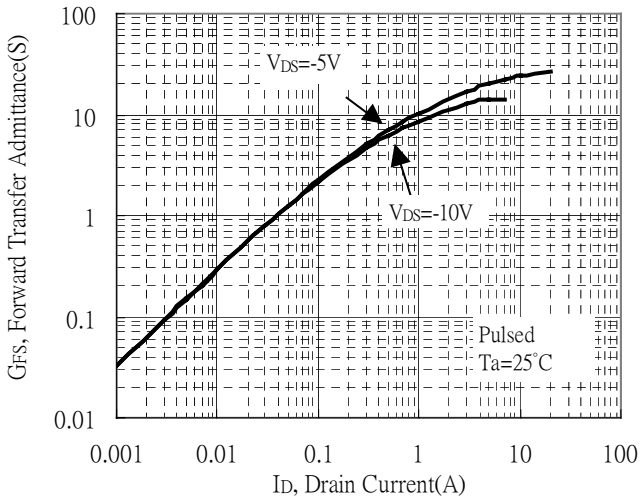
Capacitance vs Drain-to-Source Voltage



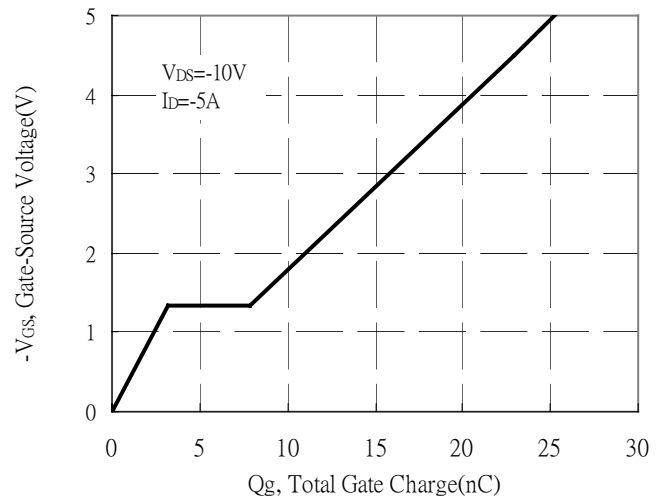
Threshold Voltage vs Junction Temperature



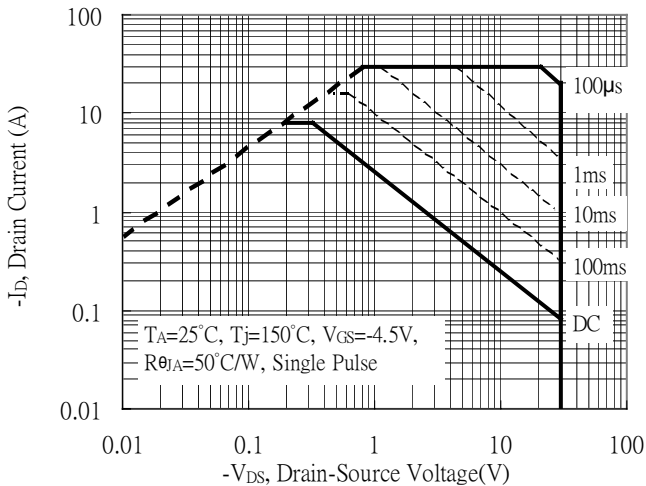
Forward Transfer Admittance vs Drain Current



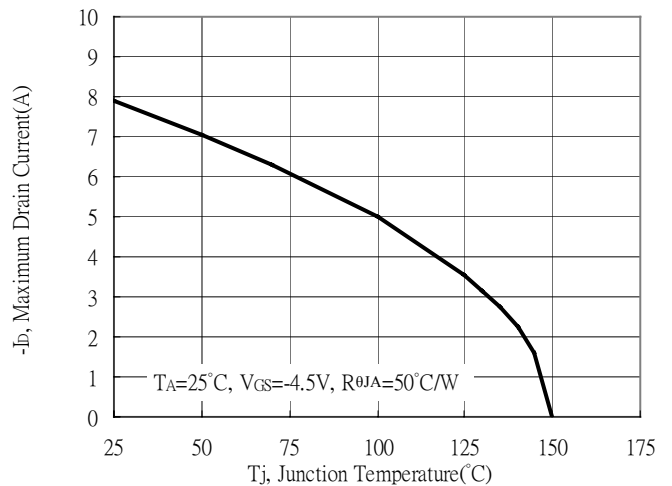
Gate Charge Characteristics



Maximum Safe Operating Area



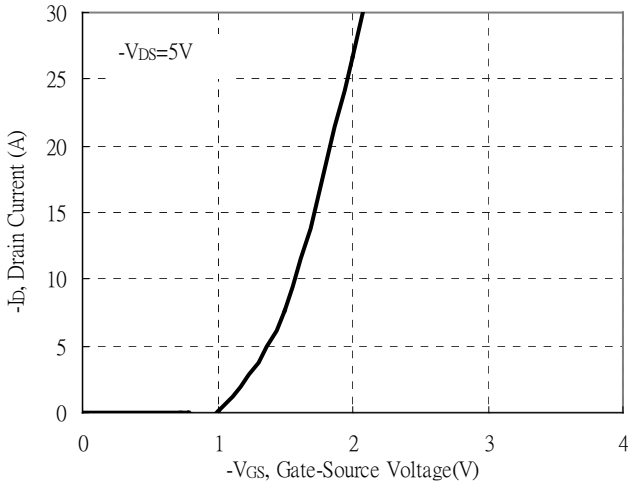
Maximum Drain Current vs Junction Temperature



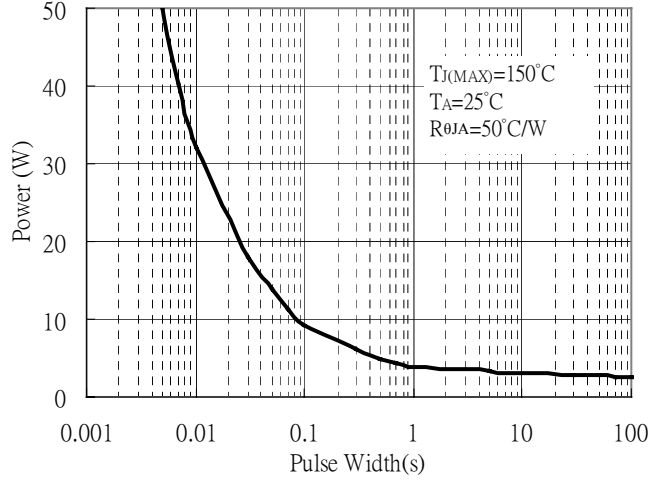


**Typical Characteristics(Cont.) : Q2(P-channel)**

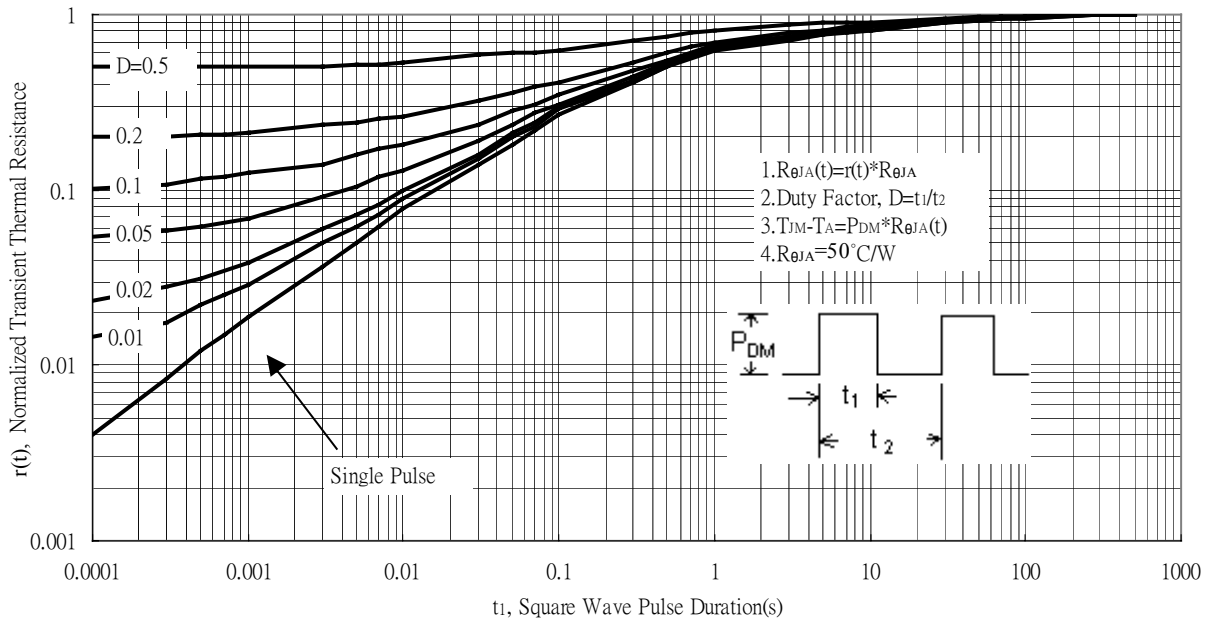
Typical Transfer Characteristics



Single Pulse Power Rating, Junction to Ambient  
 (Note on page 2)

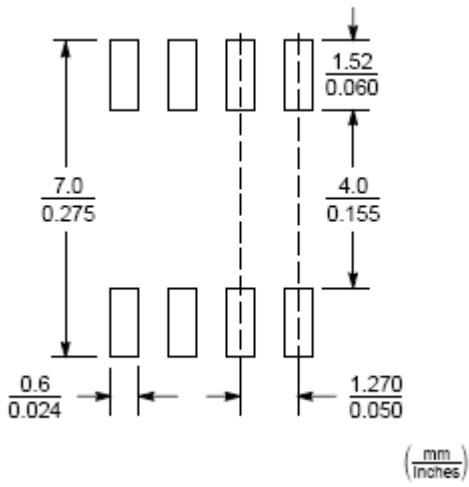


Transient Thermal Response Curves

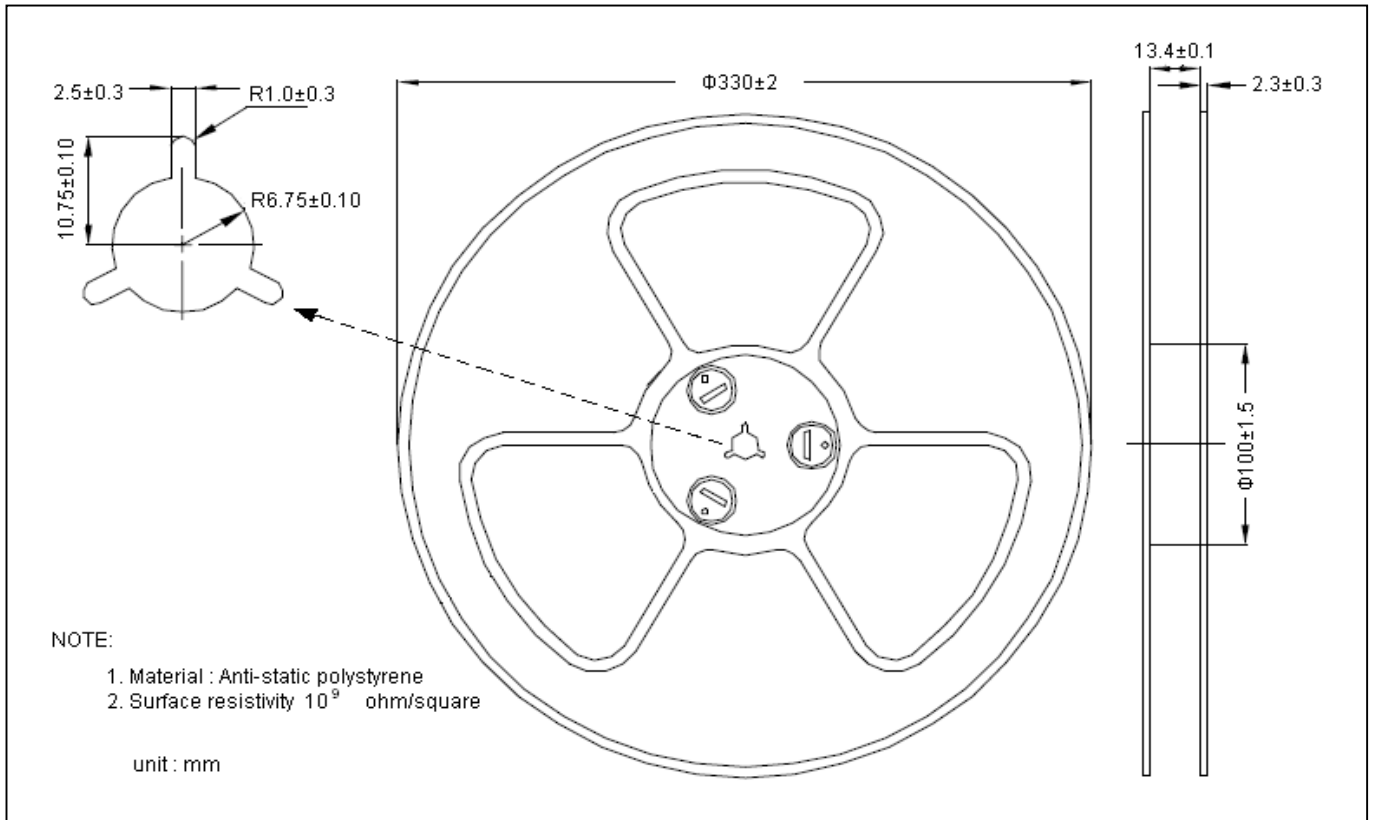




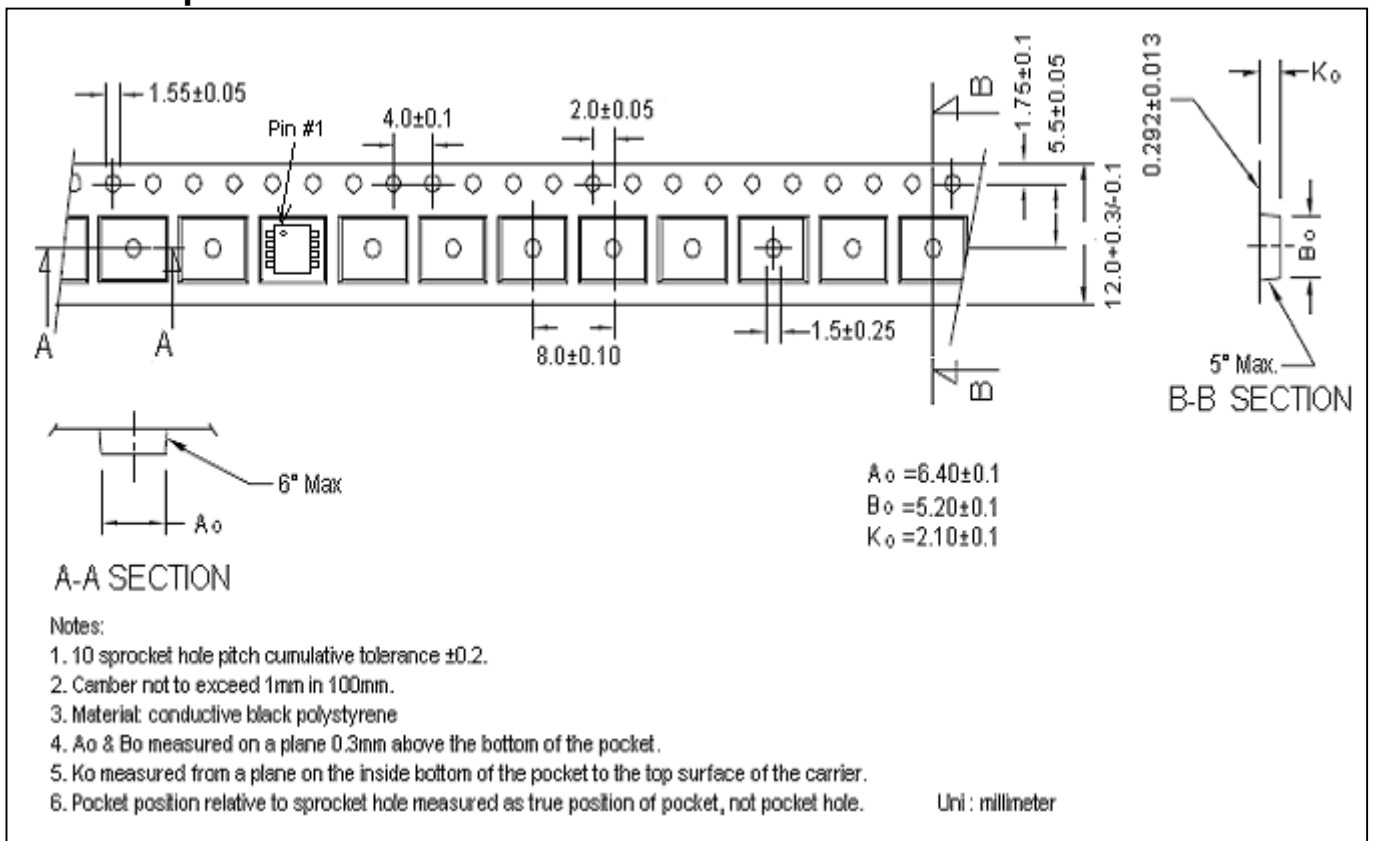
### Recommended Soldering Footprint



**Reel Dimension**



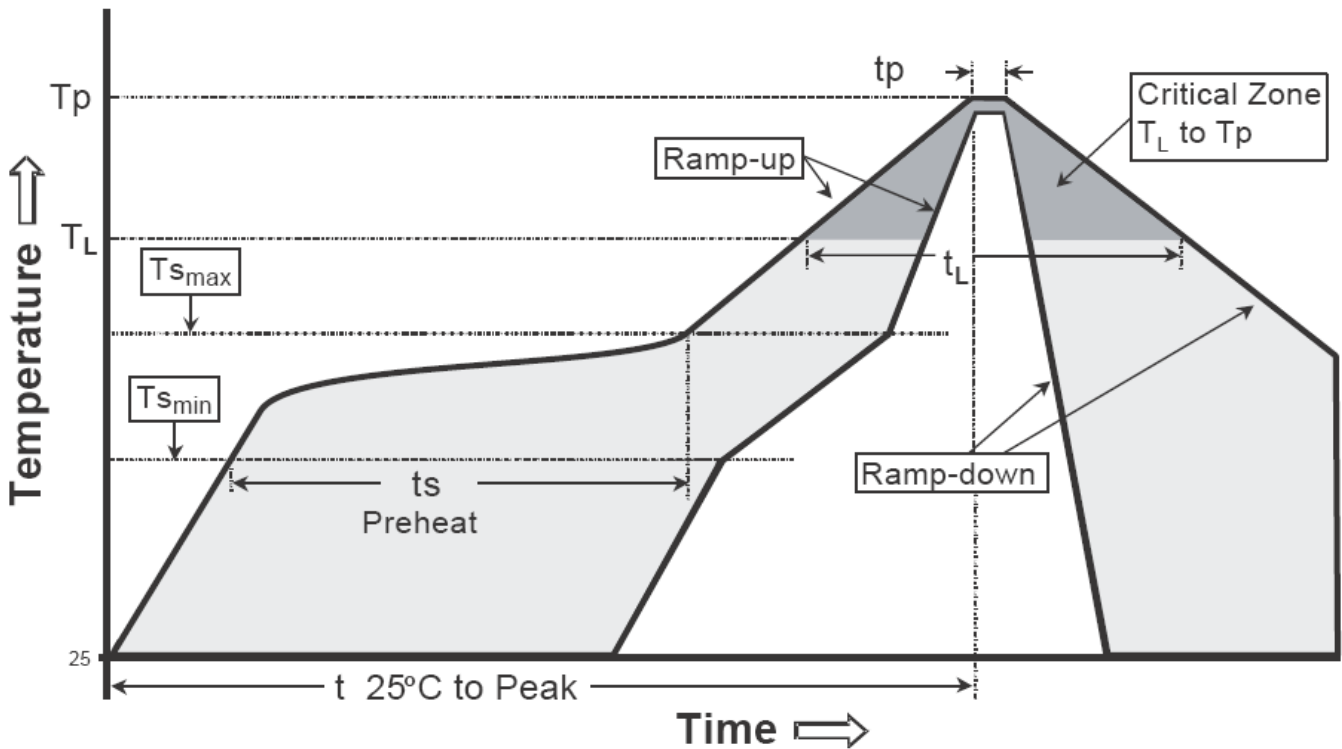
**Carrier Tape Dimension**



**Recommended wave soldering condition**

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

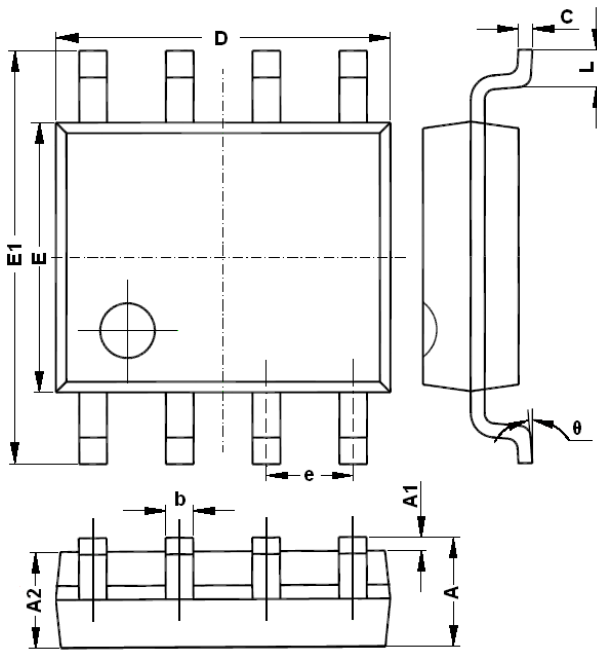
**Recommended temperature profile for IR reflow**



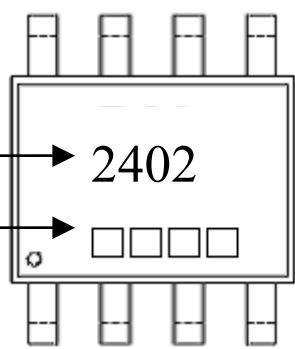
Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (TL)	183°C	217°C
- Time (tL)	60-150 seconds	60-150 seconds
Peak Temperature(Tp)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note :1. All temperatures refer to topside of the package, measured on the package body surface.  
 2.For devices mounted on FR-4 PCB of 1.6mm or equivalent grade PCB. If other grade PCB is used, care should be taken to match the coefficients of thermal expansion between components and PCB. If they are not matched well, the solder joints may crack or the bodies of the parts may crack or shatter as the assembly cools.

**Dimension**



**Marking:**



Device Name → **2402**

Date Code → [ ] [ ] [ ] [ ]

Date Code(counting from left to right) :

1<sup>st</sup> code : year code, the last digit of Christian year

2<sup>nd</sup> code : month code, Jan→A, Feb→B, Mar→C, Apr→D  
 May→E, Jun→F, Jul→G, Aug→H, Sep→J,  
 Oct→K, Nov→L, Dec→M

3<sup>rd</sup> and 4<sup>th</sup> codes : production serial number, 01~99

**8-Lead SOP-8 Plastic Package**  
 CYStek Package Code: Q8

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069	E	3.800	4.200	0.150	0.165
A1	0.100	0.250	0.004	0.010	E1	5.800	6.200	0.228	0.244
A2	1.350	1.550	0.053	0.061	e	1.270	(BSC)	0.050	(BSC)
b	0.330	0.510	0.013	0.020	L	0.300	1.270	0.012	0.050
c	0.170	0.250	0.006	0.010	θ	0	8°	0	8°
D	4.700	5.100	0.185	0.200					

**Notes:** 1.Controlling dimension: millimeters.  
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.  
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

**Material:**

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

**Important Notice:**

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.