

N-Channel Enhancement Mode Power MOSFET

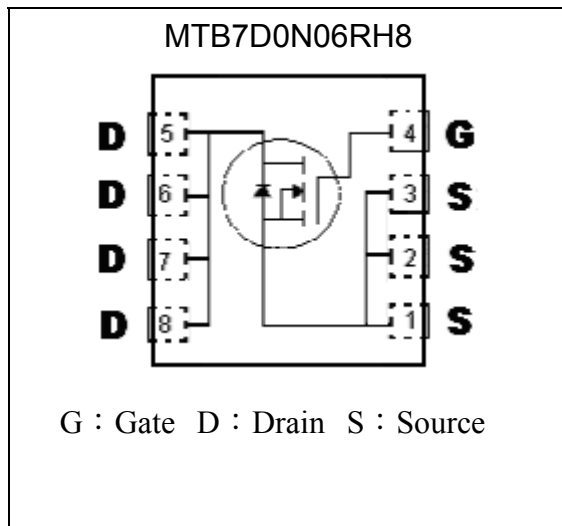
MTB7D0N06RH8

BV_{DSS}	60V
I_D@V_{GS}=10V, T_C=25°C	52A
I_D@V_{GS}=10V, T_A=25°C	12A
R_{DS(ON)}@V_{GS}=10V, I_D=20A	5.1mΩ (typ)
R_{DS(ON)}@V_{GS}=4.5V, I_D=18A	9.2mΩ (typ)

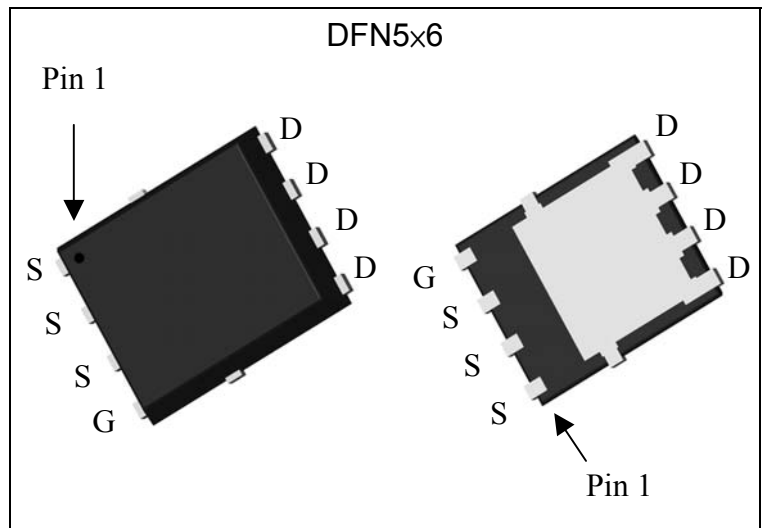
Features

- Low On Resistance
- Simple Drive Requirement
- Low Gate Charge
- Fast Switching Characteristic
- Pb-free lead plating and Halogen-free package

Symbol

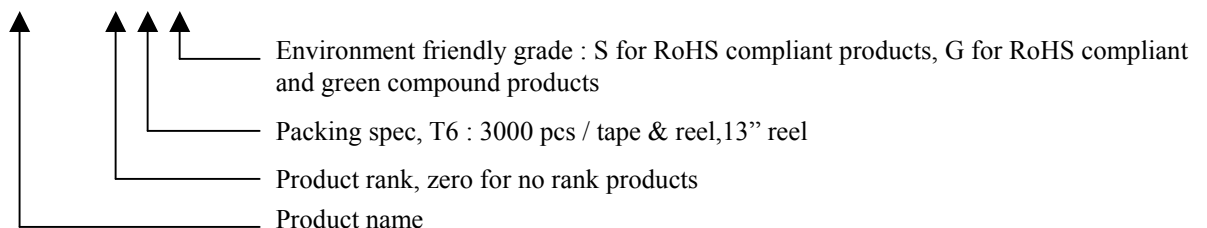


Outline



Ordering Information

Device	Package	Shipping
MTB7D0N06RH8-0-T6-G	DFN 5 ×6 (Pb-free lead plating and halogen-free package)	3000 pcs / tape & reel



**Absolute Maximum Ratings** ($T_C=25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Limits	Unit	
Drain-Source Voltage	V_{DS}	60	V	
Gate-Source Voltage	V_{GS}	± 20		
Continuous Drain Current @ $T_C=25^\circ\text{C}$, $V_{GS}=10\text{V}$ (Note 5)	I_D	52	A	
Continuous Drain Current @ $T_C=100^\circ\text{C}$, $V_{GS}=10\text{V}$ (Note 5)		32.9		
Continuous Drain Current @ $T_A=25^\circ\text{C}$, $V_{GS}=10\text{V}$ (Note 2)	I_{DSM}	12		
Continuous Drain Current @ $T_A=70^\circ\text{C}$, $V_{GS}=10\text{V}$ (Note 2)		9.6		
Pulsed Drain Current @ $V_{GS}=10\text{V}$ (Note 3)	I_{DM}	208		
Avalanche Current @ $L=0.1\text{mH}$ (Note 3)	I_{AS}	52		
Single Pulse Avalanche Energy @ $L=1\text{mH}$, $I_D=20\text{Amps}$, $V_{DD}=30\text{V}$ (Note 4)	E_{AS}	200		mJ
Repetitive Avalanche Energy (Note 3)	E_{AR}	5		
Power Dissipation	P_D	$T_C=25^\circ\text{C}$ (Note 1)	50	W
		$T_C=100^\circ\text{C}$ (Note 1)	20	
	P_{DSM}	$T_A=25^\circ\text{C}$ (Note 2)	2.5	
		$T_A=70^\circ\text{C}$ (Note 2)	1.6	
Operating Junction and Storage Temperature	T_j, T_{stg}	-55~+150	$^\circ\text{C}$	

*Drain current limited by maximum junction temperature

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	$R_{\theta JC}$	2.5	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-ambient, max (Note 2)	$R_{\theta JA}$	50	

- Note :
- The power dissipation P_D is based on $T_{J(MAX)}=150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
 - The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2 oz. copper, in a still air environment with $T_A=25^\circ\text{C}$. The value in any given application depends on the user's specific board design. The power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C .
 - Pulse width limited by junction temperature $T_{J(MAX)}=150^\circ\text{C}$.
 - Ratings are based on low frequency and low duty cycles to keep initial $T_J=25^\circ\text{C}$. 100% tested by conditions of $V_{DD}=25\text{V}$, $I_D=20\text{A}$, $L=0.1\text{mH}$, $V_{GS}=10\text{V}$.
 - Calculated continuous drain current based on maximum allowable junction temperature.
 - The static characteristics are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% maximum.
 - The $R_{\theta JA}$ is the sum of thermal resistance from junction to case $R_{\theta JC}$ and case to ambient.

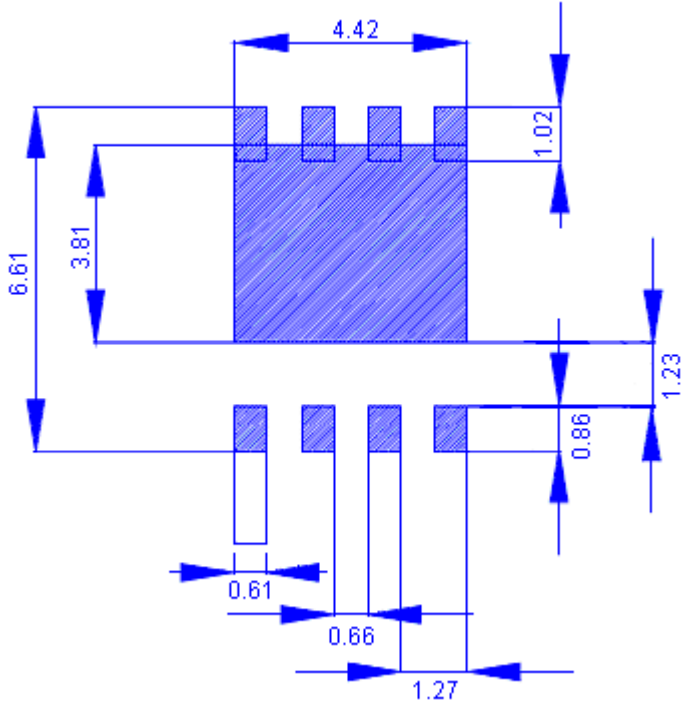


Characteristics (Tj=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	60	-	-	V	V _{GS} =0V, I _D =250μA
ΔBV _{DSS} /ΔT _j	-	0.03	-	V/°C	Reference to 25°C, I _D =250μA
V _{GS(th)}	1	-	2.5	V	V _{DS} = V _{GS} , I _D =250μA
*G _{FS}	-	23	-	S	V _{DS} =10V, I _D =20A
I _{GSS}	-	-	±100	nA	V _{GS} =±20V, V _{DS} =0V
I _{DSS}	-	-	1	μA	V _{DS} =48V, V _{GS} =0V
	-	-	5		V _{DS} =48V, V _{GS} =0V, T _j =55°C
*R _{DS(ON)}	-	5.1	7	mΩ	V _{GS} =10V, I _D =20A
	-	9.2	13		V _{GS} =4.5V, I _D =18A
Dynamic					
*Q _g	-	46.8	-	nC	V _{DS} =48V, I _D =20A, V _{GS} =10V
*Q _{gs}	-	9.7	-		
*Q _{gd}	-	9.5	-		
*t _{d(ON)}	-	19.4	-	ns	V _{DS} =30V, I _D =20A, V _{GS} =10V, R _G =3Ω
*t _r	-	17	-		
*t _{d(OFF)}	-	54.2	-		
*t _f	-	9.6	-		
C _{iss}	-	2931	-	pF	V _{GS} =0V, V _{DS} =30V, f=1MHz
C _{oss}	-	375	-		
C _{rss}	-	17	-		
R _g	-	1.7	-	Ω	f=1MHz
Source-Drain Diode					
*I _S	-	-	52	A	
*I _{SM}	-	-	208		
*V _{SD}	-	0.86	1.2	V	I _S =20A, V _{GS} =0V
*t _{rr}	-	23	-	ns	V _{GS} =0, I _F =20A, dI _F /dt=100A/μs
*Q _{rr}	-	18.5	-	nC	

*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

Recommended Soldering Footprint

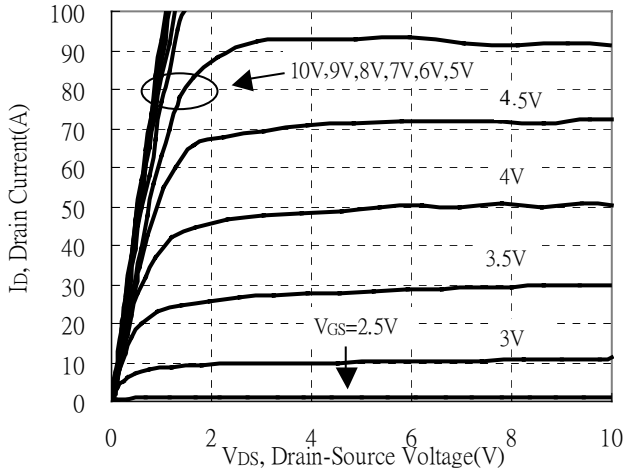


unit : mm

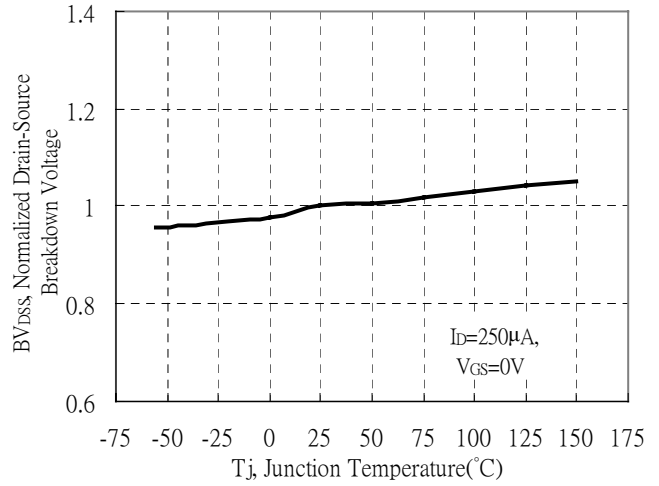


Typical Characteristics

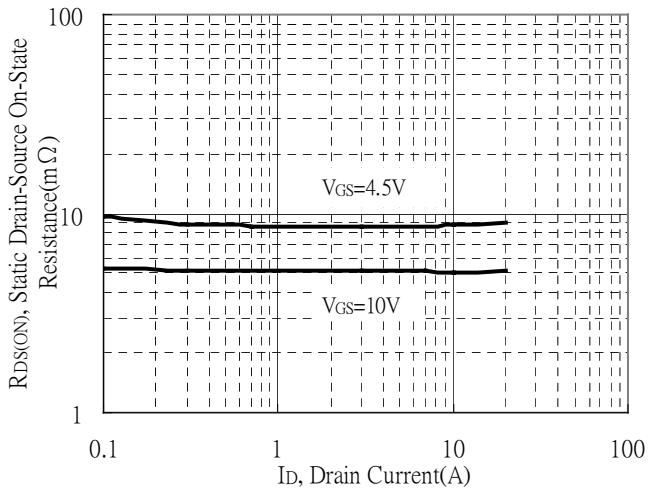
Typical Output Characteristics



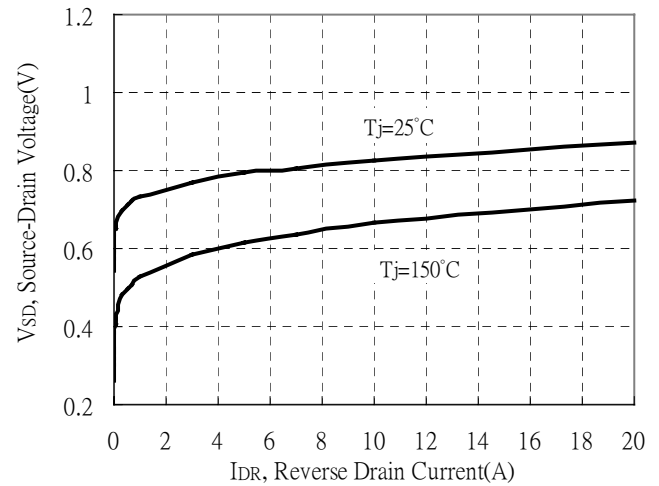
Brekdown Voltage vs Ambient Temperature



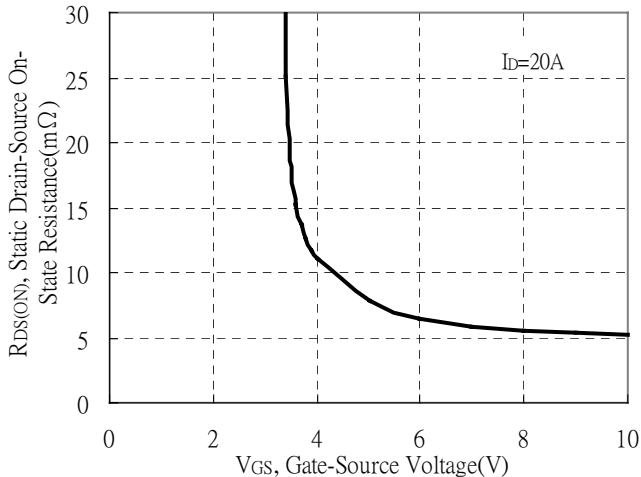
Static Drain-Source On-State resistance vs Drain Current



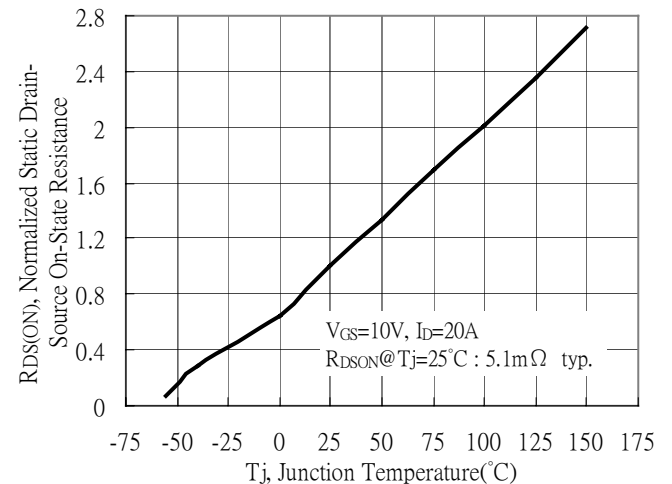
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

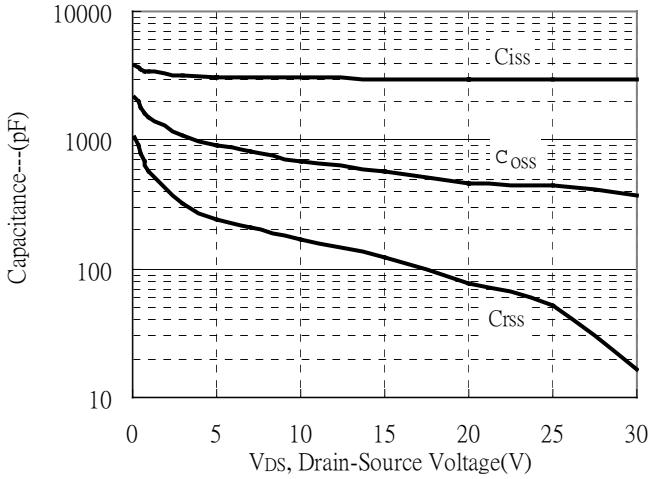


Drain-Source On-State Resistance vs Junction Temperature

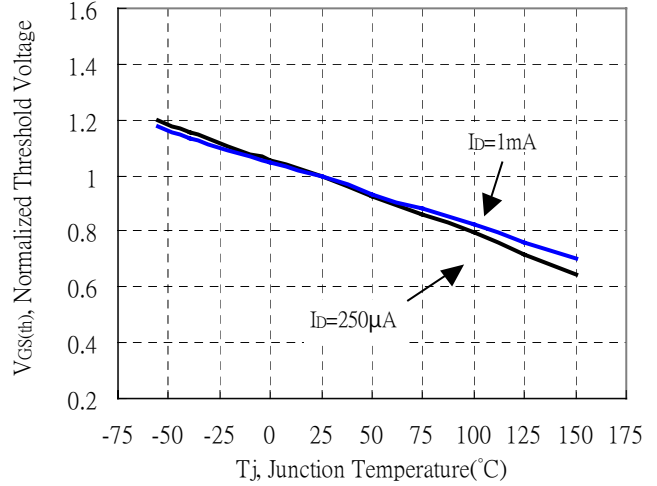


Typical Characteristics(Cont.)

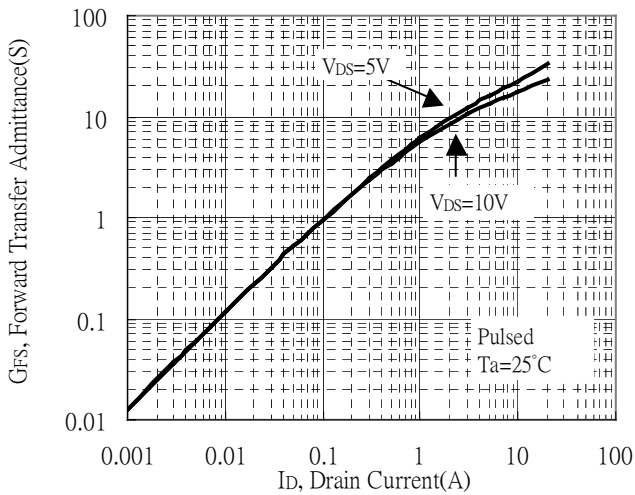
Capacitance vs Drain-to-Source Voltage



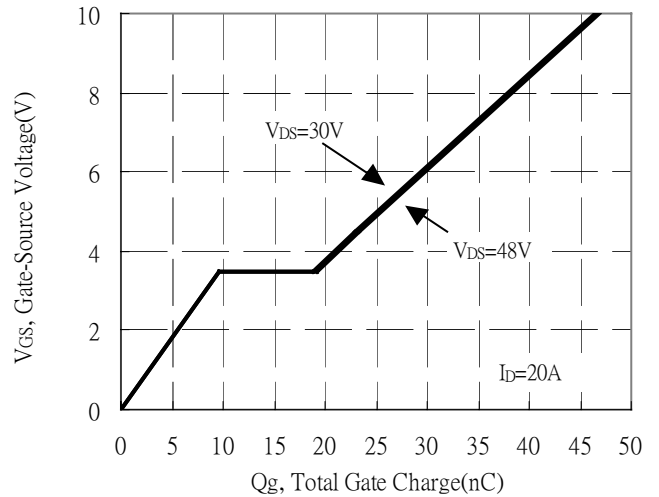
Threshold Voltage vs Junction Temperature



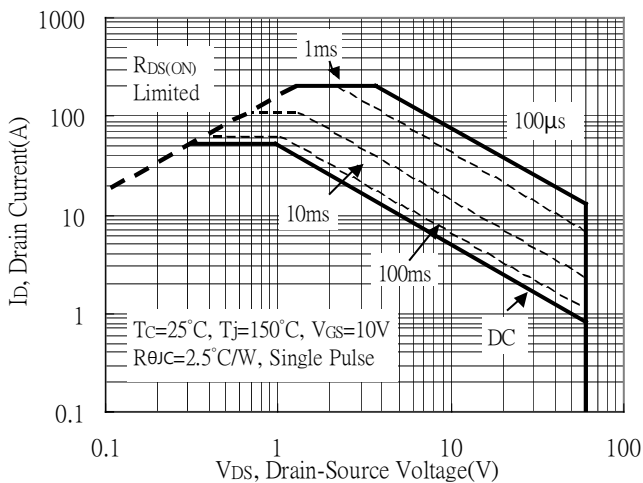
Forward Transfer Admittance vs Drain Current



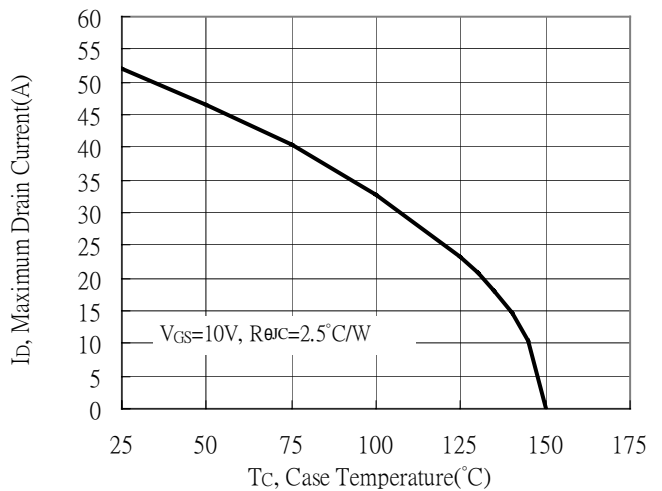
Gate Charge Characteristics



Maximum Safe Operating Area



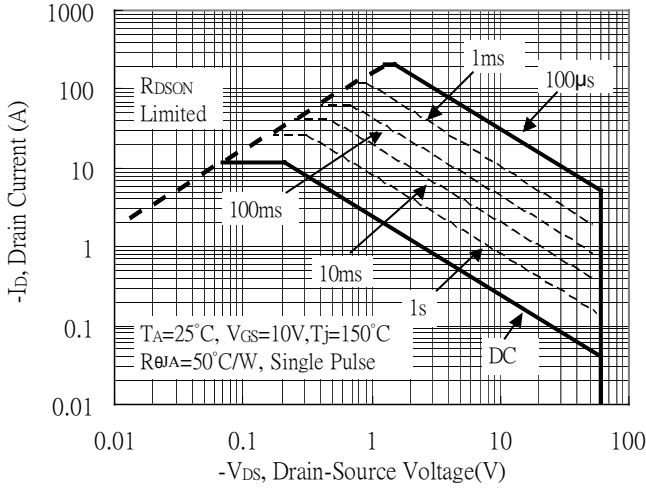
Maximum Drain Current vs Case Temperature



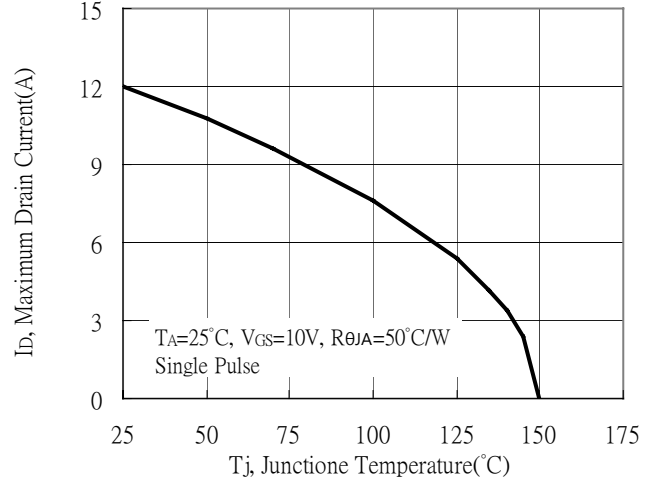


Typical Characteristics(Cont.)

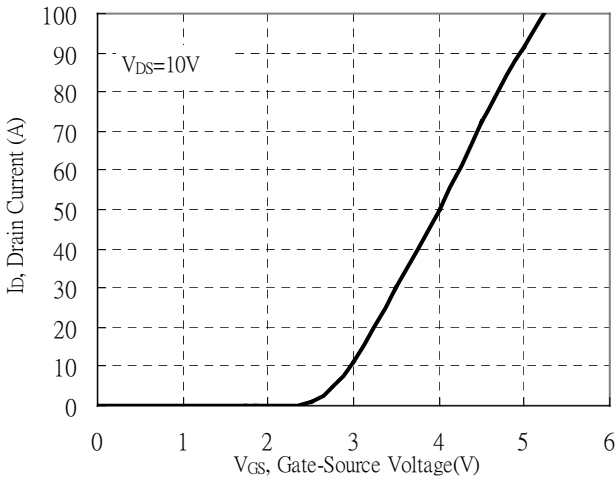
Maximum Safe Operating Area



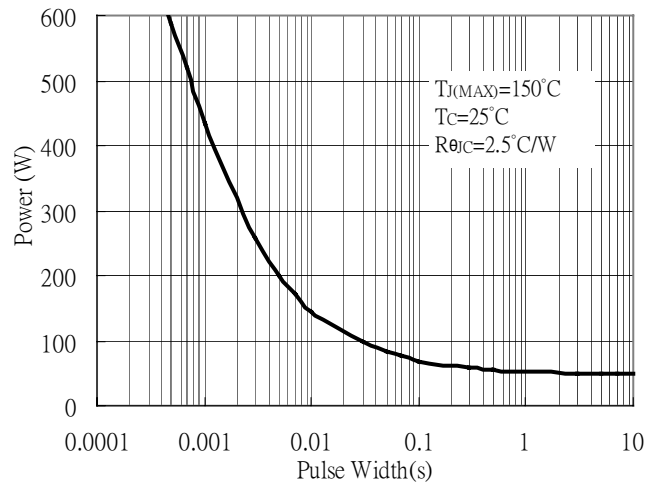
Maximum Drain Current vs Junction Temperature



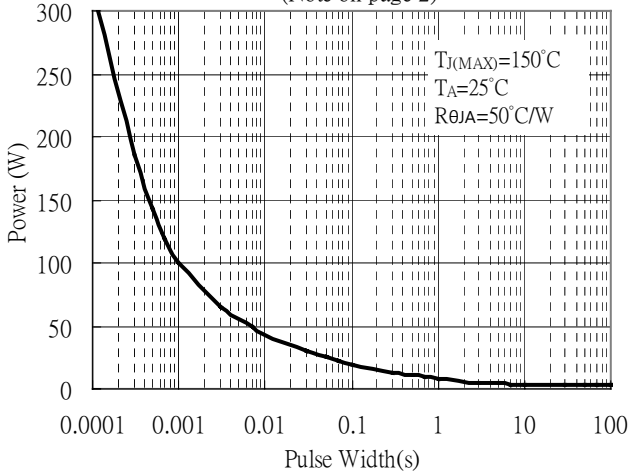
Typical Transfer Characteristics



Single Pulse Maximum Power Dissipation

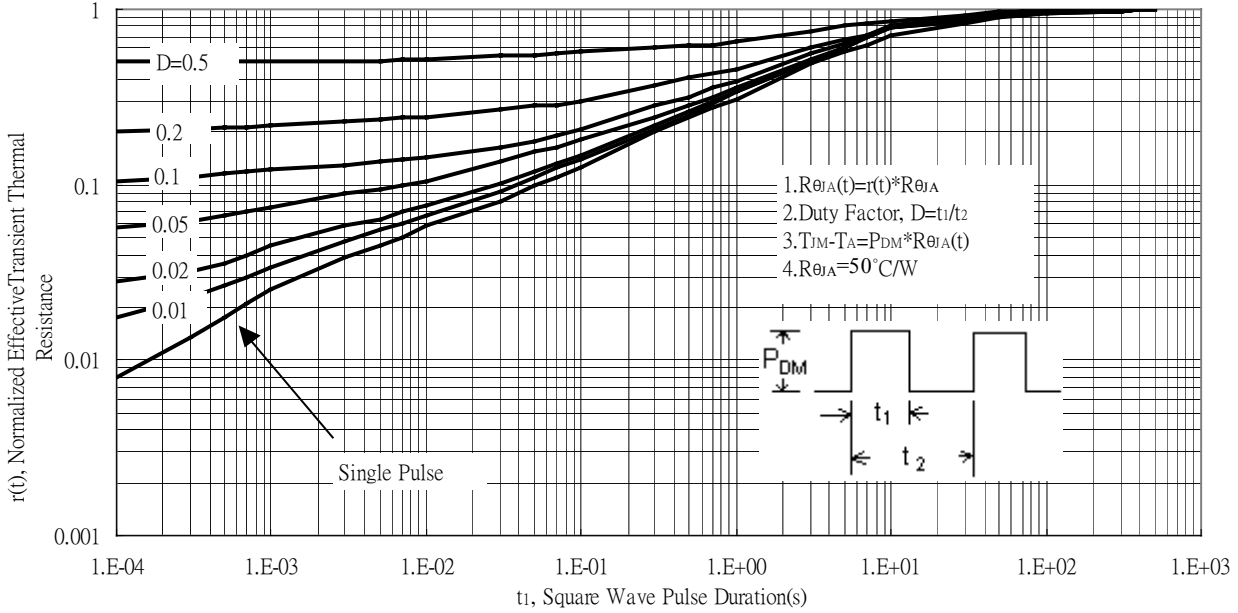


Single Pulse Power Rating, Junction to Ambient
 (Note on page 2)

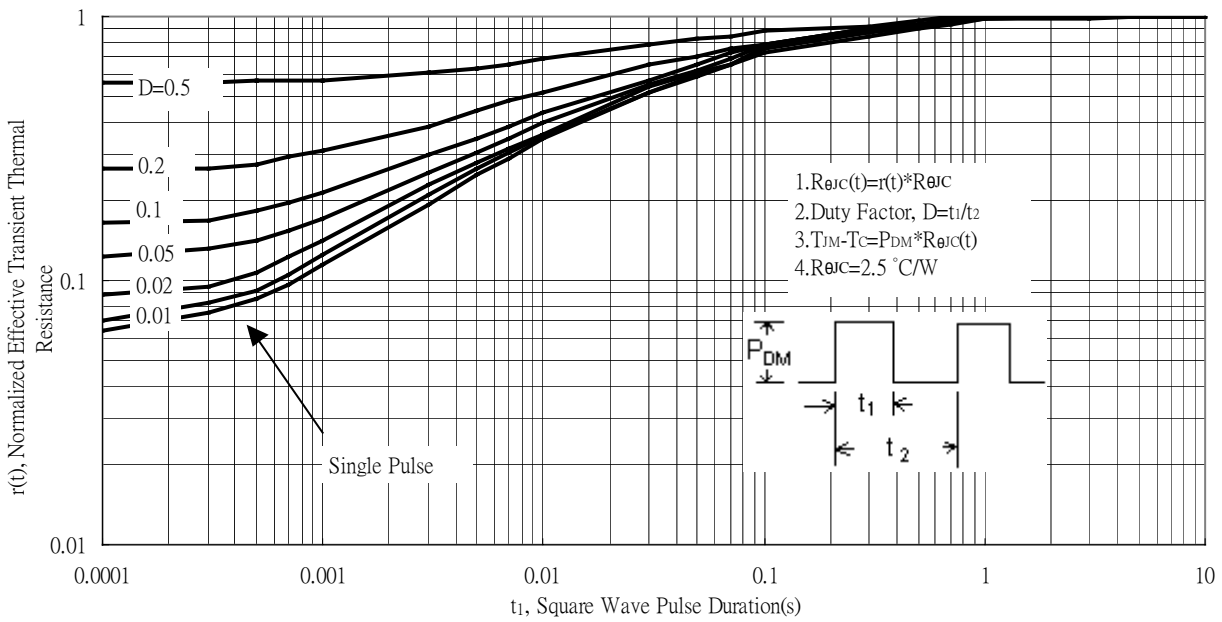


Typical Characteristics(Cont.)

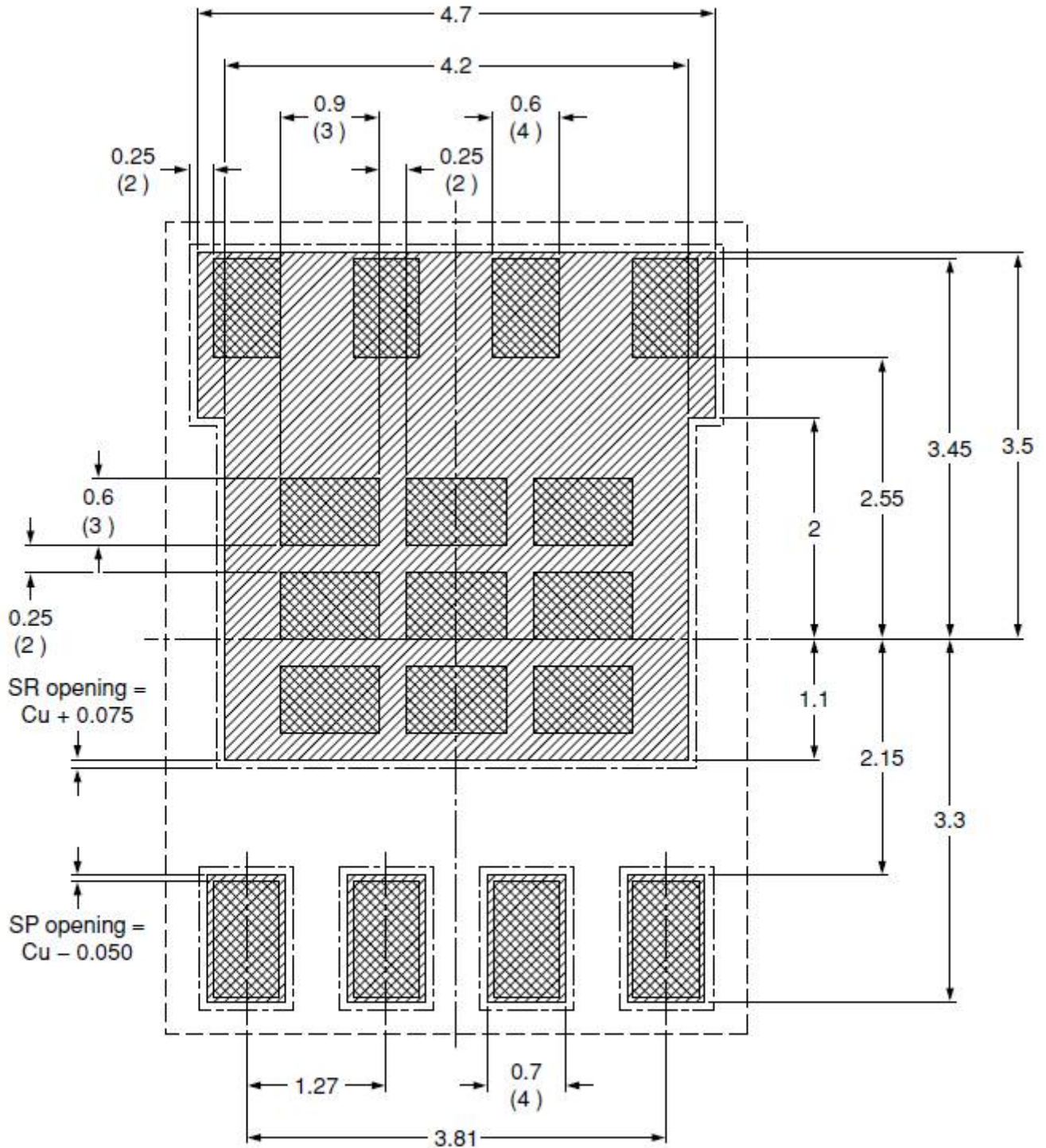
Transient Thermal Response Curves



Transient Thermal Response Curves



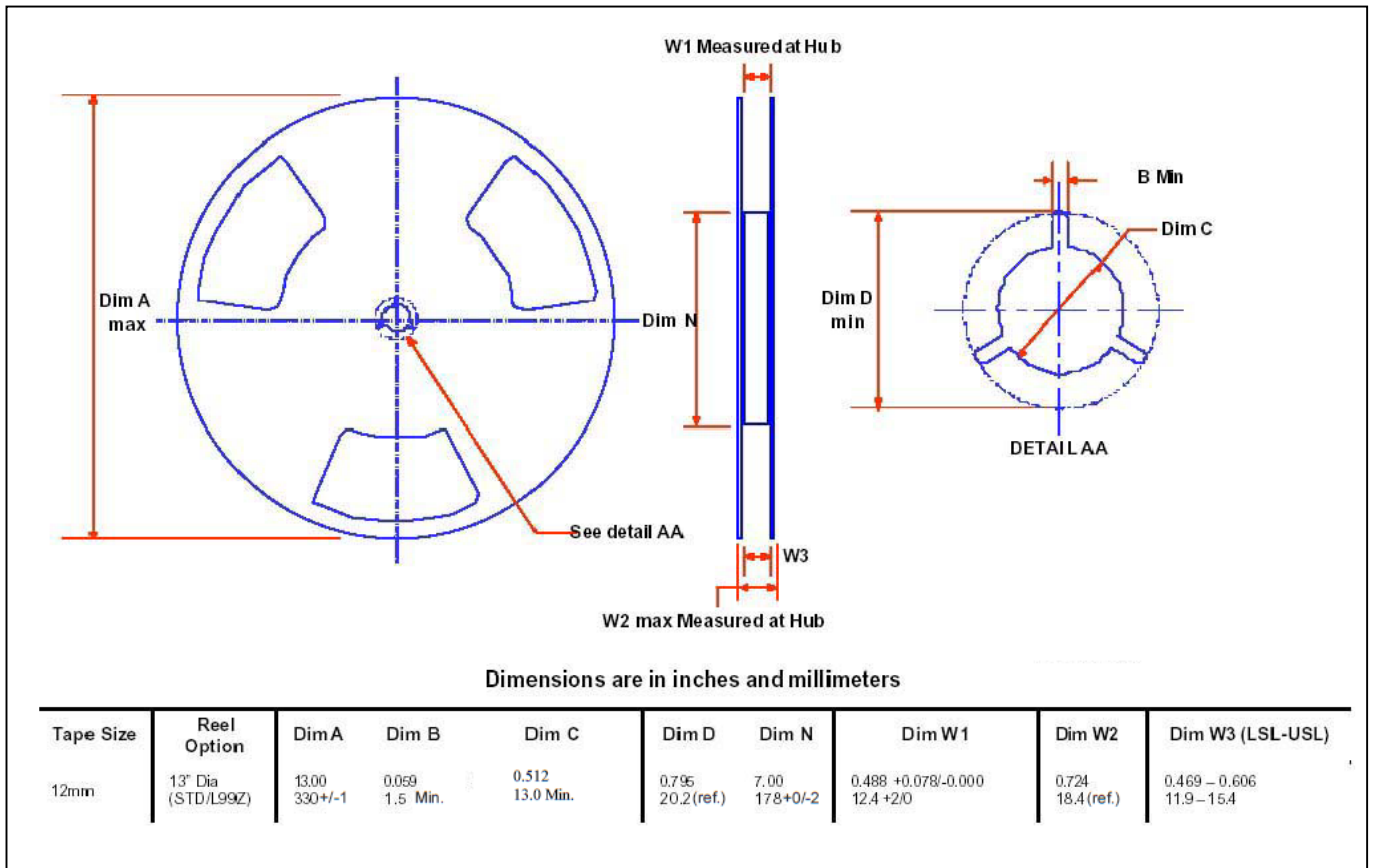
Recommended Soldering Footprint & Stencil Design



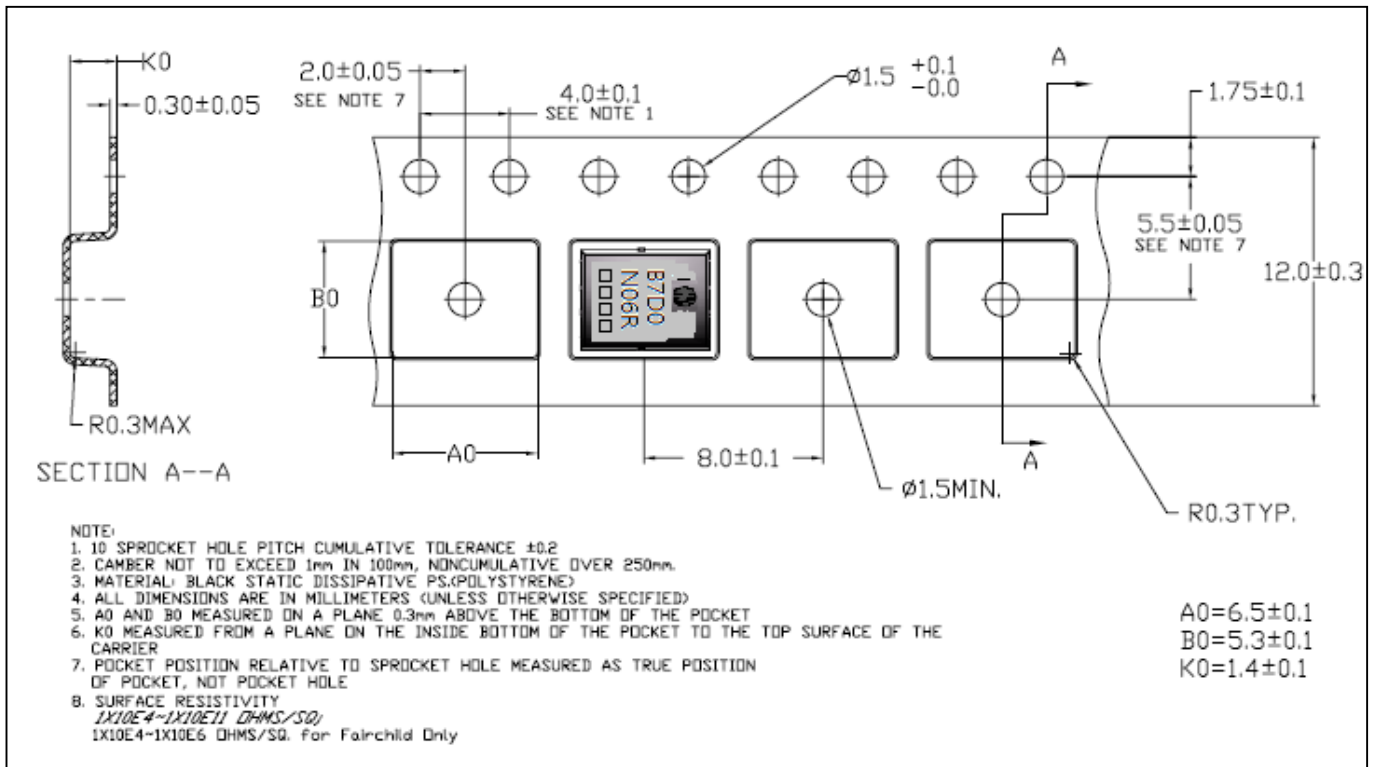
- | | |
|---|--|
|  solder lands |  solder paste
125 μm stencil |
|  solder resist |  occupied area |

unit : mm

Reel Dimension



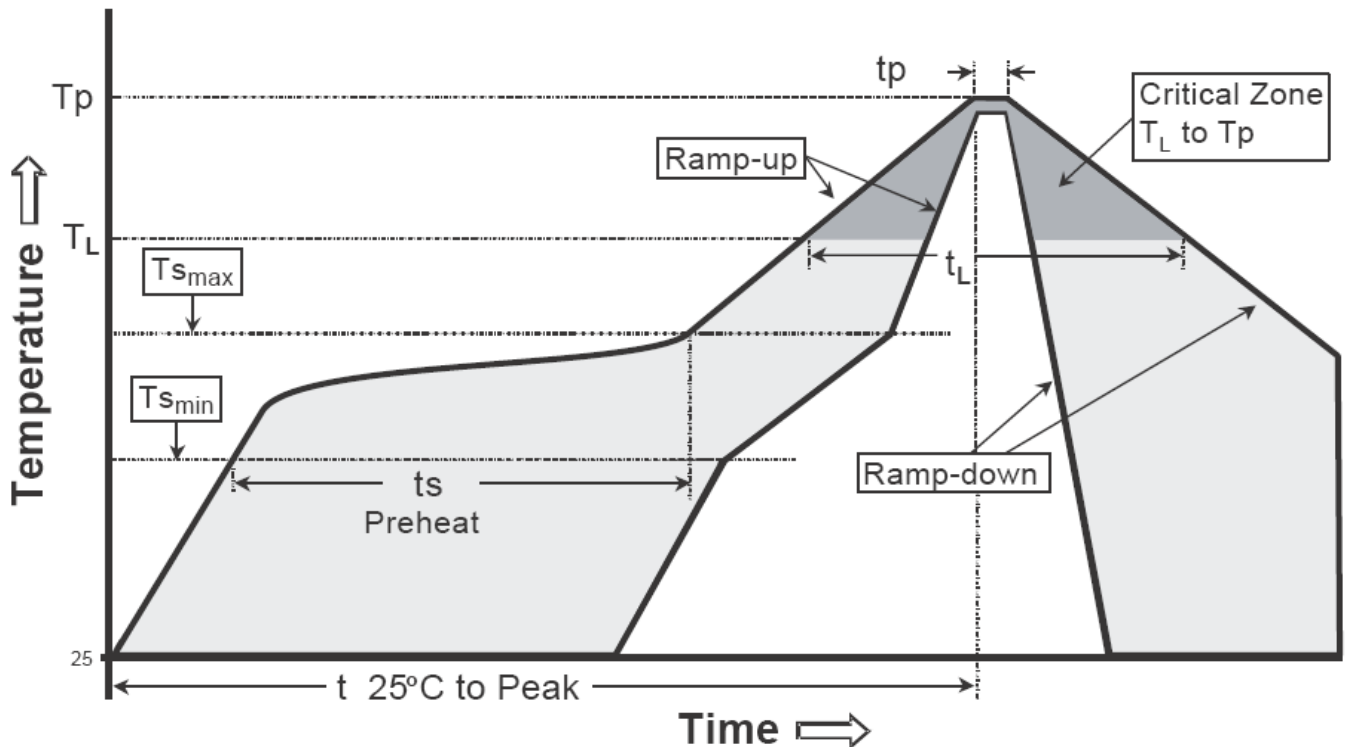
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

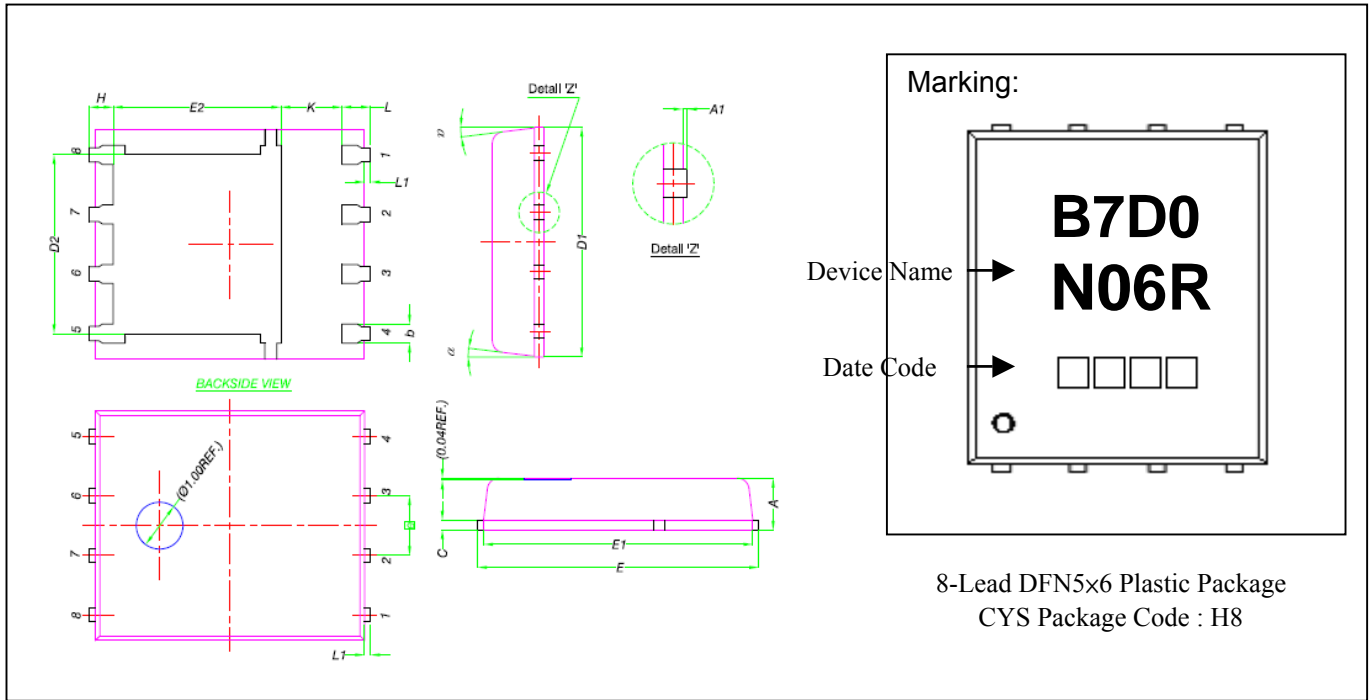
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _p)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(t _p)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note :1. All temperatures refer to topside of the package, measured on the package body surface.
 2.For devices mounted on FR-4 PCB of 1.6mm or equivalent grade PCB. If other grade PCB is used, care should be taken to match the coefficients of thermal expansion between components and PCB. If they are not matched well, the solder joints may crack or the bodies of the parts may crack or shatter as the assembly cools.

DFN5x6 Dimension



DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.90	1.10	0.035	0.043	E2	3.38	3.78	0.133	0.149
A1	0.00	0.05	0.000	0.002	e	1.27 BSC		0.050 BSC	
b	0.33	0.51	0.013	0.020	H	0.41	0.61	0.016	0.024
C	0.20	0.30	0.008	0.012	K	1.10	-	0.043	-
D1	4.80	5.00	0.189	0.197	L	0.51	0.71	0.020	0.028
D2	3.61	3.96	0.142	0.156	L1	0.06	0.20	0.002	0.008
E	5.90	6.10	0.232	0.240	θ	8°	12°	8°	12°
E1	5.70	5.80	0.224	0.228					

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.