

N-Channel Logic Level Enhancement Mode Power MOSFET

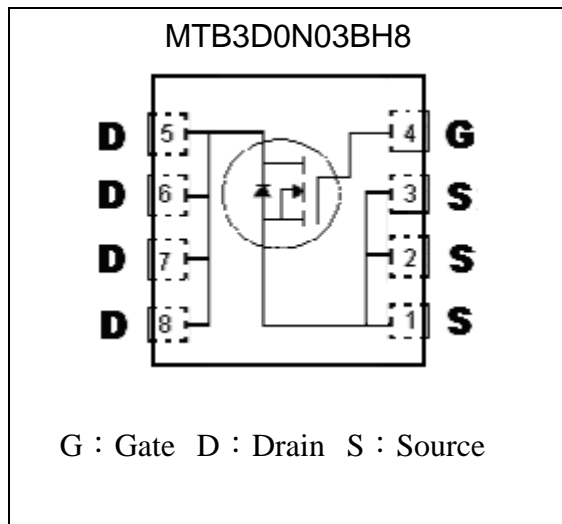
MTB3D0N03BH8

| | |
|------------------------------------------------------------------|---------------------|
| BV_{DSS} | 30V |
| I_D@V_{GS}=10V, T_C=25°C | 60A |
| I_D@V_{GS}=10V, T_A=25°C | 19.2A |
| R_{DS(ON)}@V_{GS}=10V, I_D=30A | 2.5 mΩ (typ) |
| R_{DS(ON)}@V_{GS}=4.5V, I_D=24A | 3.5 mΩ (typ) |

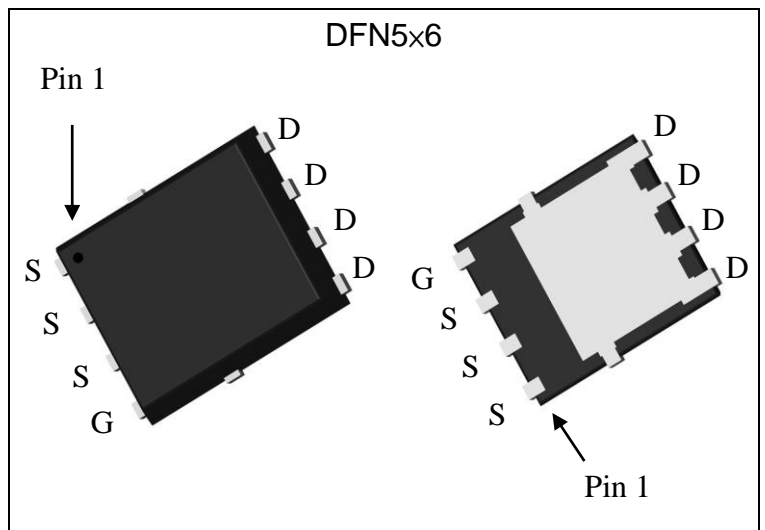
Features

- Single Drive Requirement
- Low On-resistance
- Fast Switching Characteristic
- Pb-free lead plating and Halogen-free package

Symbol

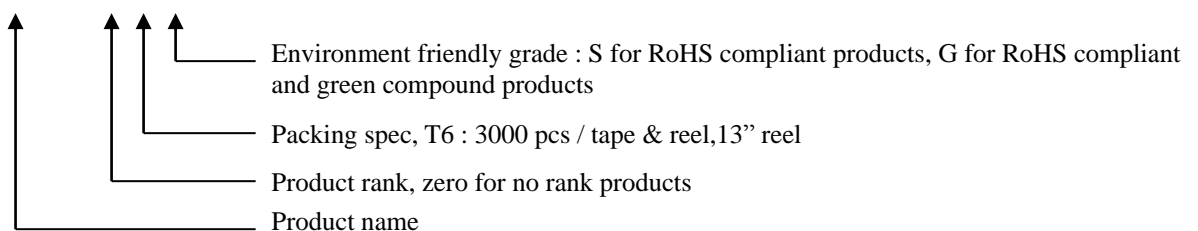


Outline



Ordering Information

| Device | Package | Shipping |
|---------------------|-------------------------------------------------------------|------------------------|
| MTB3D0N03BH8-0-T6-G | DFN 5 ×6 (Pb-free lead plating and halogen-free package) | 3000 pcs / tape & reel |





Absolute Maximum Ratings (Ta=25°C)

| Parameter | Symbol | Limits | Unit | |
|---------------------------------------------------------------------------------------|-----------------------------------|-----------------------|--------|---|
| Drain-Source Voltage | V _{DS} | 30 | V | |
| Gate-Source Voltage | V _{GS} | ±20 | | |
| Continuous Drain Current @ T _C =25°C, V _{GS} =10V(Silicon limit) | I _D | 86 | A | |
| Continuous Drain Current @ T _C =100°C, V _{GS} =10V(Silicon limit) | | 54 | | |
| Continuous Drain Current @ T _C =25°C, V _{GS} =10V(Package limit) | | 60 | | |
| Continuous Drain Current @ T _A =25°C, V _{GS} =10V | I _{DSM} | 19.2 *3 | | |
| Continuous Drain Current @ T _A =70°C, V _{GS} =10V | | 15.4 *3 | | |
| Pulsed Drain Current | I _{DM} | 200 *1 | | |
| Avalanche Current | I _{AS} | 46 | | |
| Avalanche Energy @ L=0.1mH, I _D =46A, R _G =25Ω | E _{AS} | 106 | mJ | |
| Total Power Dissipation | P _D | T _C =25°C | 50 | W |
| | | T _C =100°C | 20 | |
| | P _D SM | T _A =25°C | 2.5 *3 | |
| | | T _A =70°C | 1.6 *3 | |
| Operating Junction and Storage Temperature Range | T _j , T _{stg} | -55~+150 | °C | |

100% UIS testing in condition of V_D=15V, L=0.1mH, V_G=10V, I_L=30A, Rated V_{DS}=30V N-CH

Thermal Data

| Parameter | Symbol | Value | Unit |
|----------------------------------------------|---------------------|-------|------|
| Thermal Resistance, Junction-to-case, max | R _{th,j-c} | 2.5 | °C/W |
| Thermal Resistance, Junction-to-ambient, max | R _{th,j-a} | 50 *3 | |

- Note : 1. Pulse width limited by maximum junction temperature
 2. Duty cycle ≤ 1%
 3. Surface mounted on 1 in² copper pad of FR-4 board, t ≤ 10s; 125°C/W when mounted on minimum copper pad.

Characteristics (Tc=25°C, unless otherwise specified)

| Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|------------------------|------|------|------|------|------------------------------------------------------------------|
| Static | | | | | |
| BV _{DSS} | 30 | - | - | V | V _{GS} =0V, I _D =250μA |
| V _{GS(th)} | 1.0 | - | 2.5 | | V _{DS} = V _{GS} , I _D =250μA |
| G _{FS} *1 | - | 41 | - | S | V _{DS} =5V, I _D =20A |
| I _{GSS} | - | - | ±100 | nA | V _{GS} =±20V, V _{DS} =0V |
| I _{DSS} | - | - | 1 | μA | V _{DS} =24V, V _{GS} =0V |
| | - | - | 25 | | V _{DS} =20V, V _{GS} =0V, T _j =125°C |
| R _{DS(ON)} *1 | - | 2.5 | 3.5 | mΩ | V _{GS} =10V, I _D =30A |
| | - | 3.5 | 5.0 | | V _{GS} =4.5V, I _D =24A |
| Dynamic | | | | | |
| C _{iss} | - | 2355 | - | pF | V _{GS} =0V, V _{DS} =15V, f=1MHz |
| C _{oss} | - | 419 | - | | |
| C _{rss} | - | 232 | - | | |

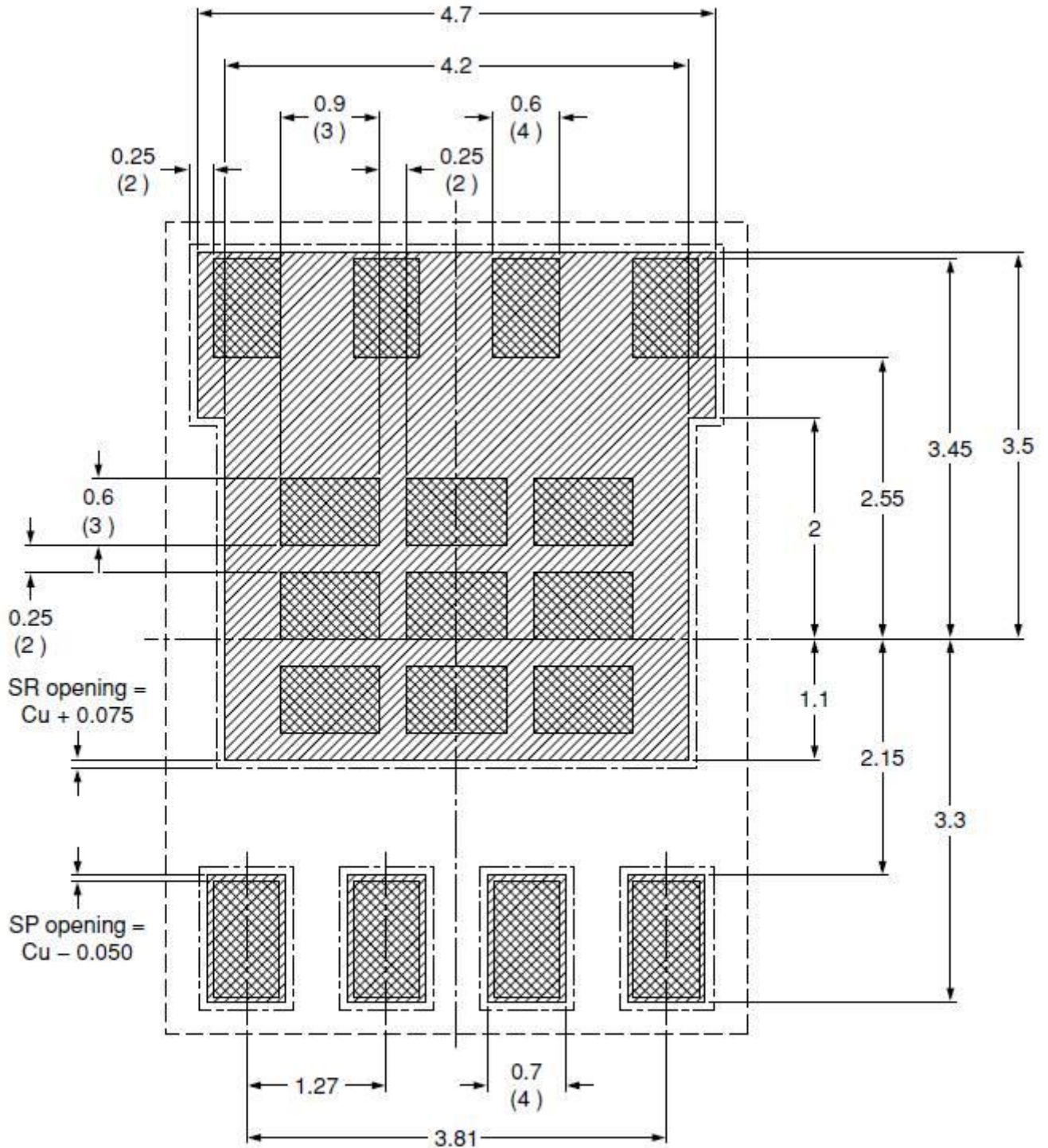




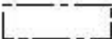

Characteristics (Tc=25°C, unless otherwise specified)

| Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---------------------------|------|------|------|------|---------------------------------------|
| Qg (VGS=10V) *1, 2 | - | 47.2 | - | nC | VDS=15V, VGS=10V, ID=30A |
| Qg (VGS=4.5V) *1, 2 | - | 24 | - | | |
| Qgs *1, 2 | - | 8.3 | - | | |
| Qgd *1, 2 | - | 10.2 | - | | |
| td(ON) *1, 2 | - | 16.4 | - | ns | VDS=15V, ID=24A, VGS=10V, RGS=2.7Ω |
| tr *1, 2 | - | 19.2 | - | | |
| td(OFF) *1, 2 | - | 53.4 | - | | |
| tf *1, 2 | - | 12.2 | - | | |
| Rg | - | 0.76 | - | Ω | f=1MHz |
| Source-Drain Diode | | | | | |
| IS *1 | - | - | 60 | A | |
| ISM *3 | - | - | 200 | | |
| VSD *1 | - | 0.81 | 1.2 | V | IS=20A, VGS=0V |
| trr | - | 16.1 | - | ns | IF=24A, dIF/dt=100A/μs |
| Qrr | - | 8.4 | - | nC | |

Note : *1.Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%
 *2.Independent of operating temperature
 *3.Pulse width limited by maximum junction temperature.

Recommended Soldering Footprint & Stencil Design



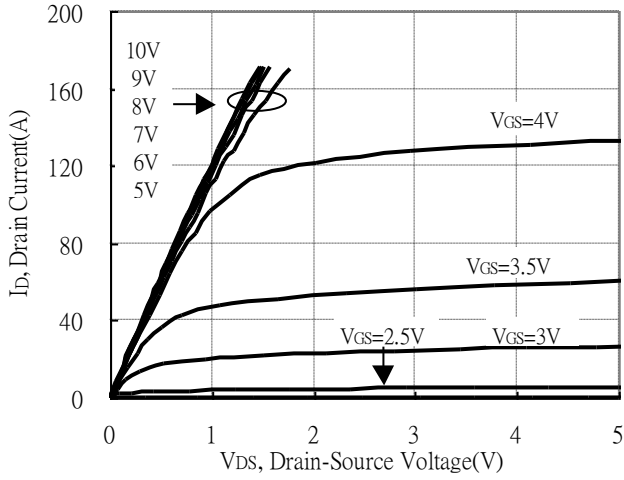
- | | |
|---------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------|
|  solder lands |  solder paste 125 μm stencil |
|  solder resist |  occupied area |

unit : mm

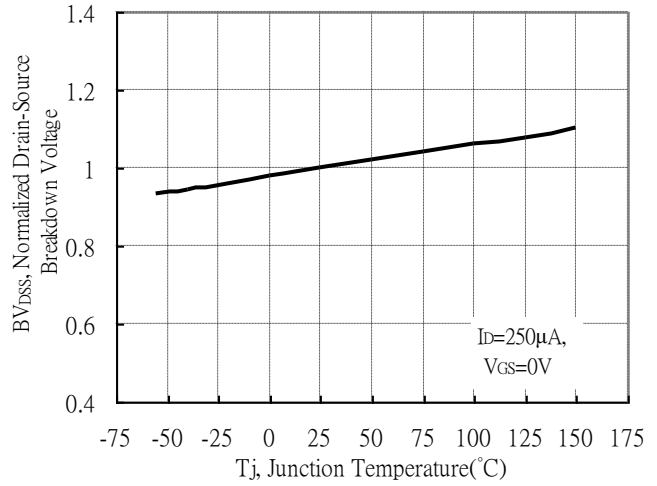


Typical Characteristics

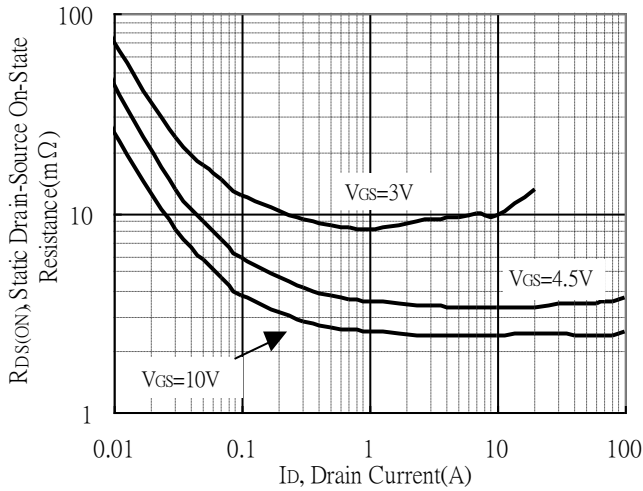
Typical Output Characteristics



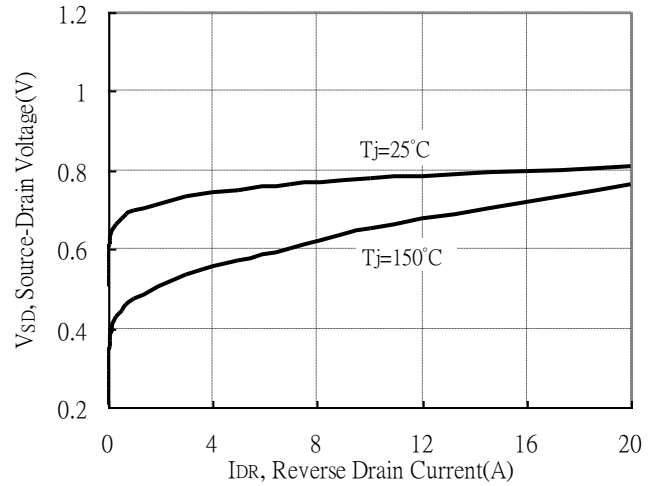
Brekdown Voltage vs Ambient Temperature



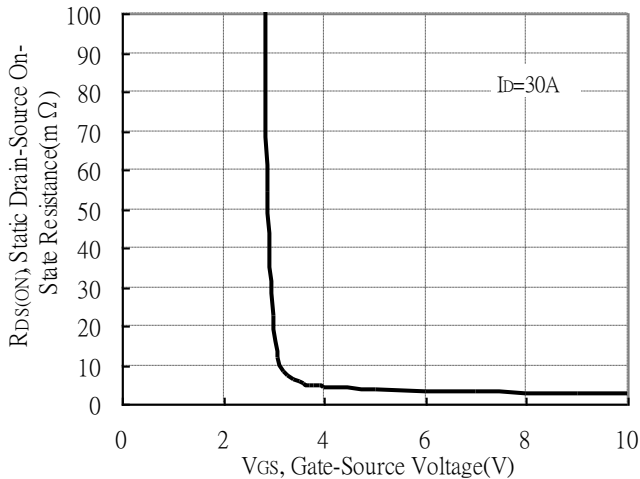
Static Drain-Source On-State resistance vs Drain Current



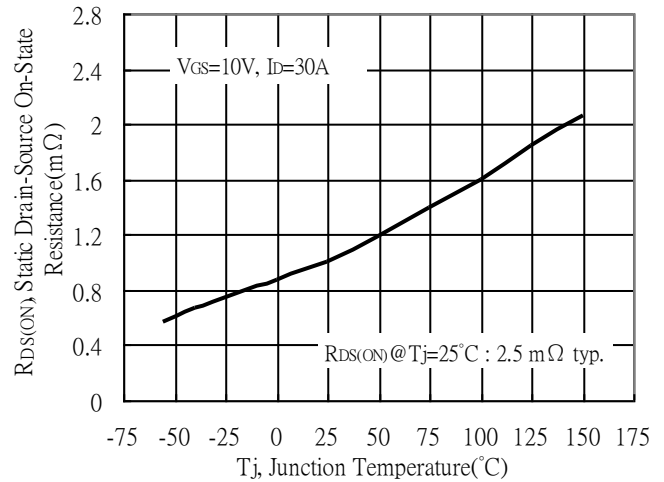
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

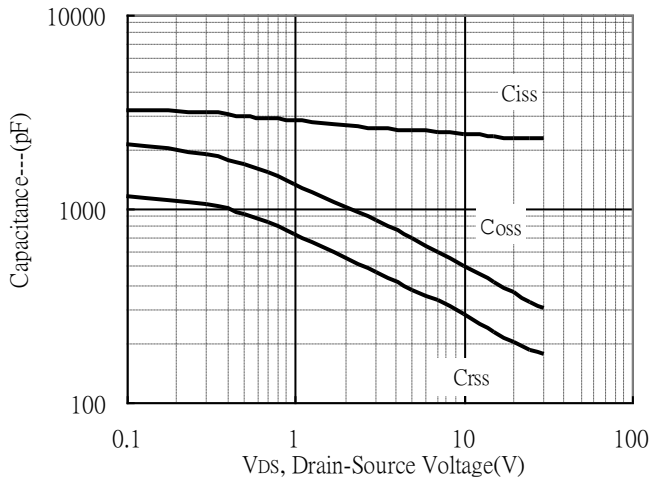


Drain-Source On-State Resistance vs Junction Temperature

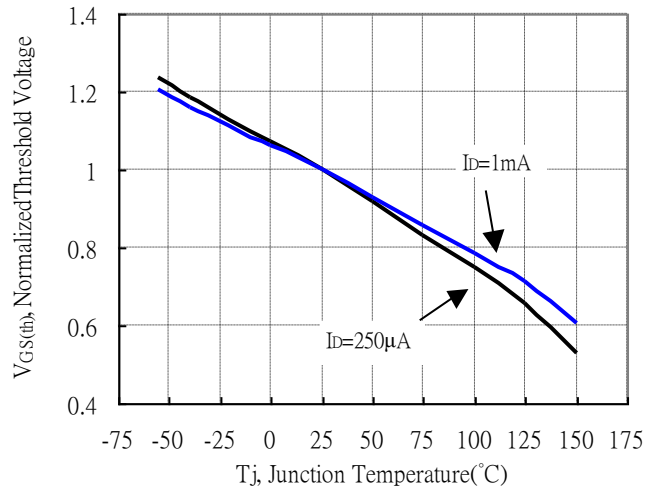


Typical Characteristics(Cont.)

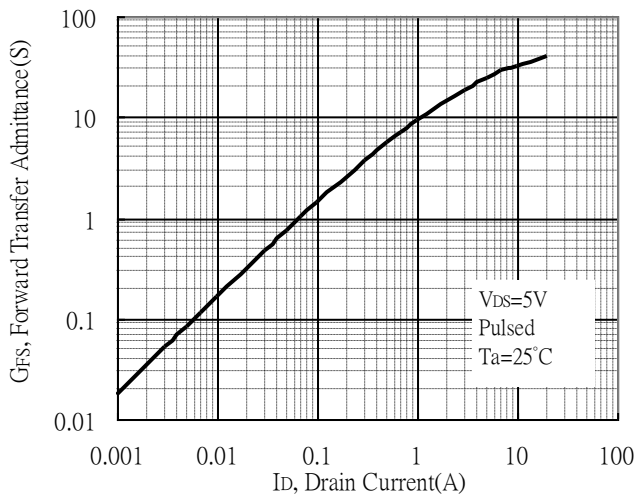
Capacitance vs Drain-to-Source Voltage



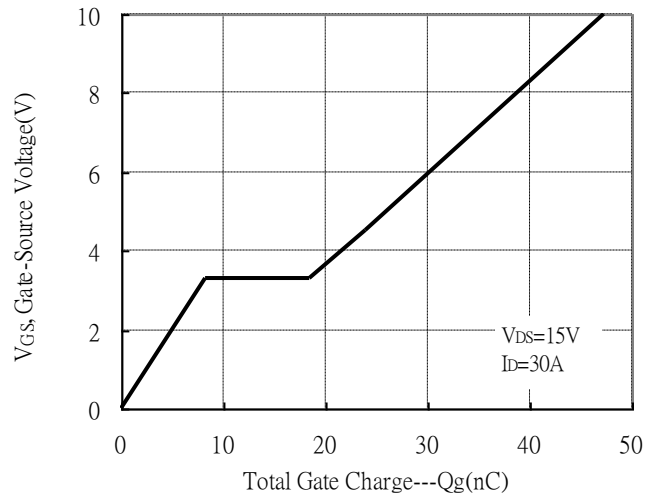
Threshold Voltage vs Junction Temperature



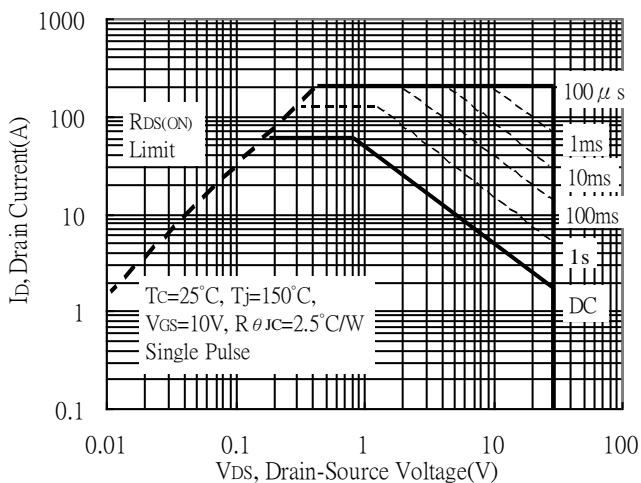
Forward Transfer Admittance vs Drain Current



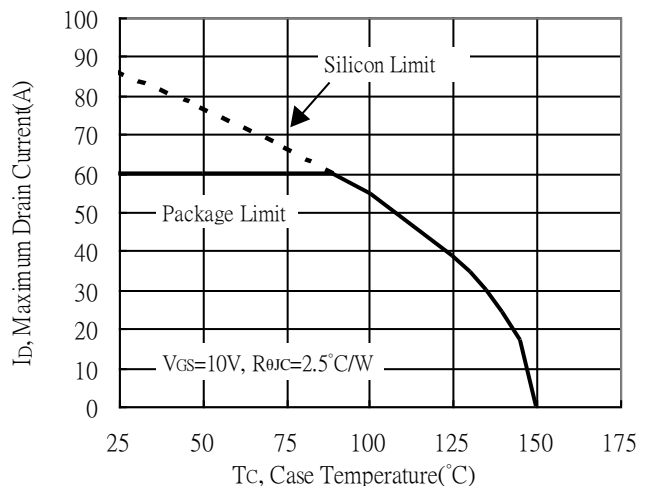
Gate Charge Characteristics



Maximum Safe Operating Area



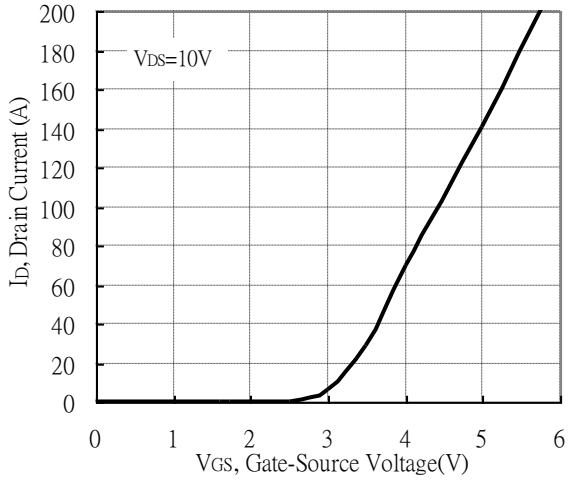
Maximum Drain Current vs Case Temperature



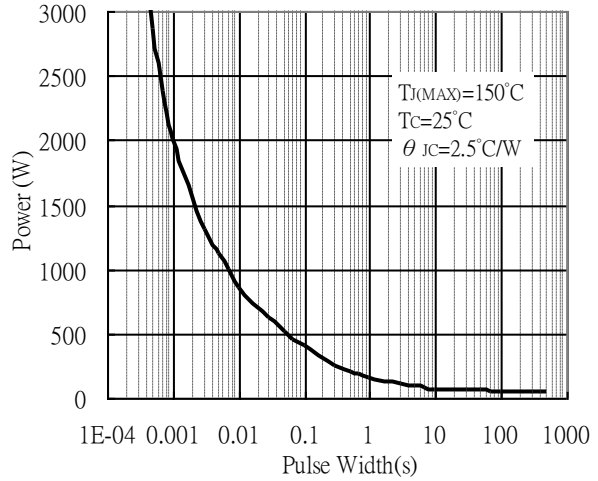


Typical Characteristics(Cont.)

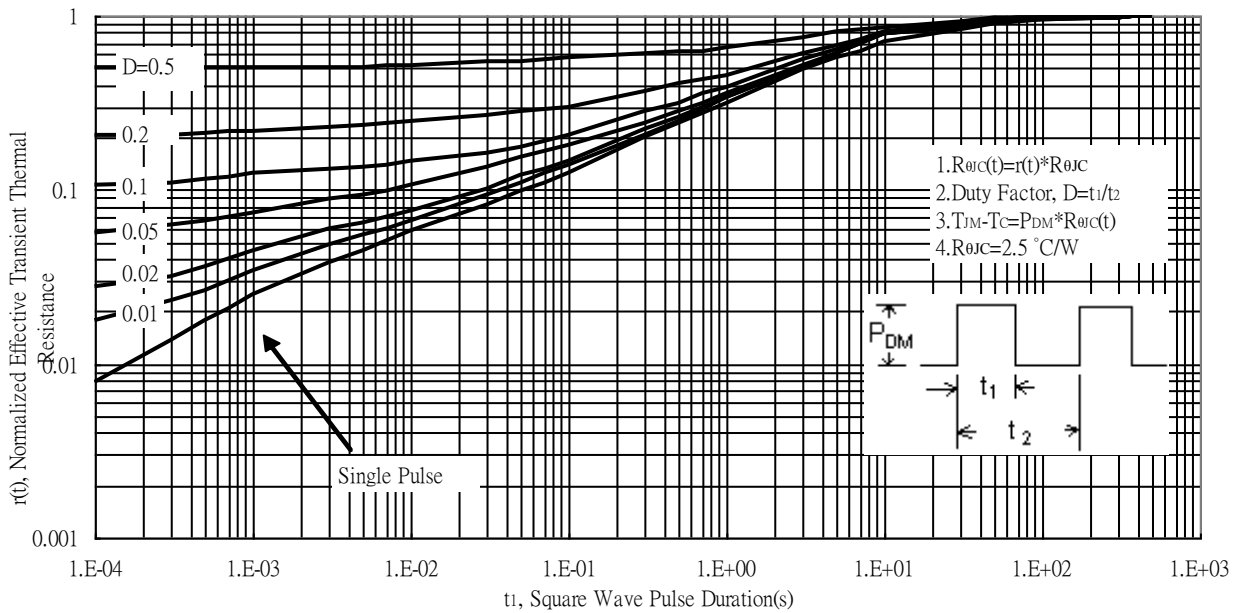
Typical Transfer Characteristics



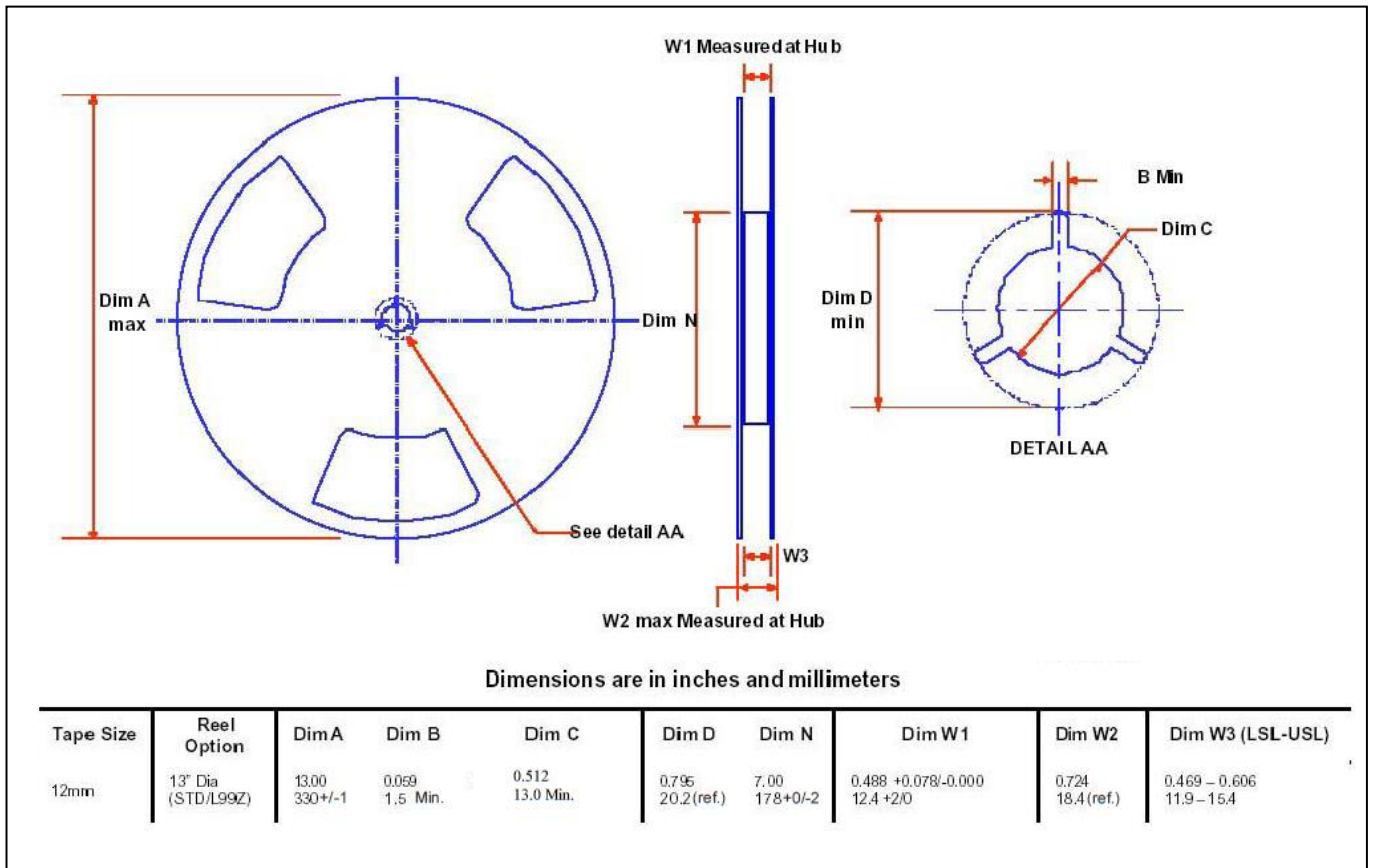
Single Pulse Maximum Power Dissipation



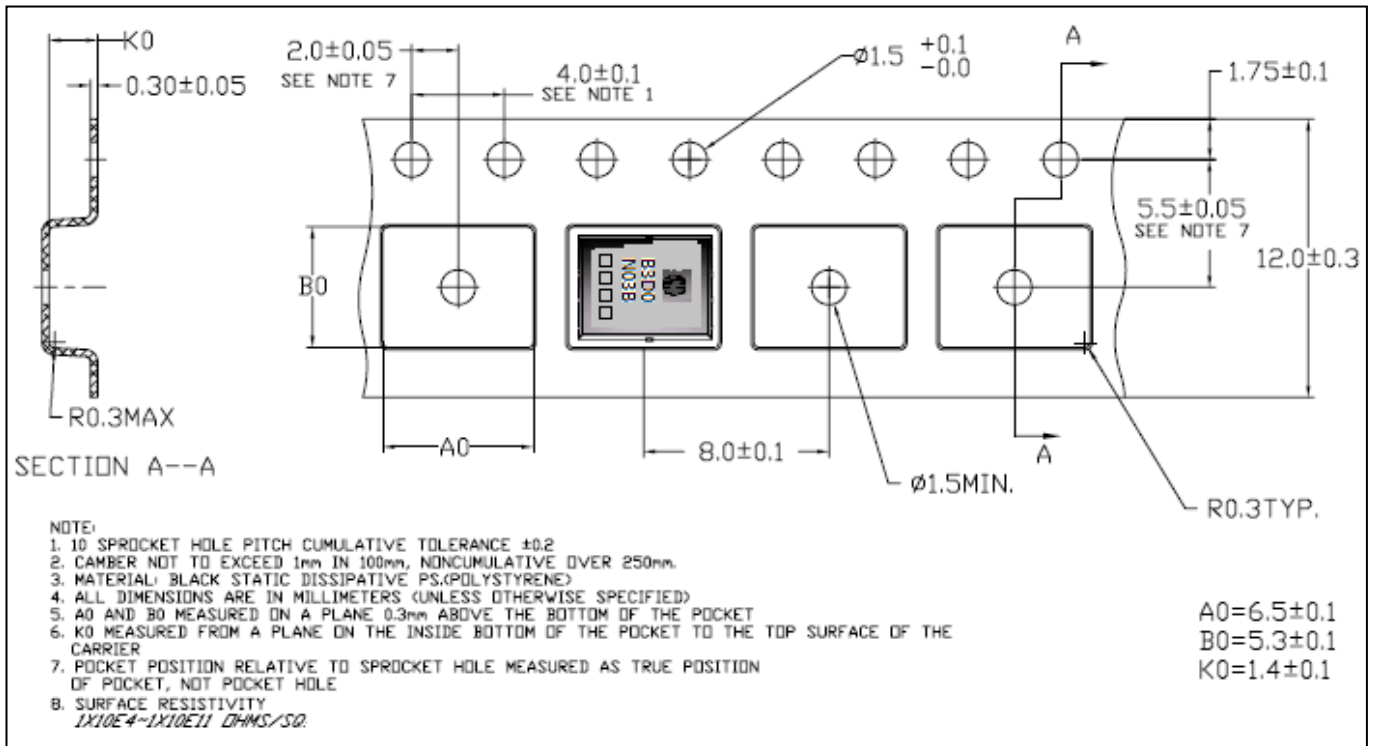
Transient Thermal Response Curves



Reel Dimension



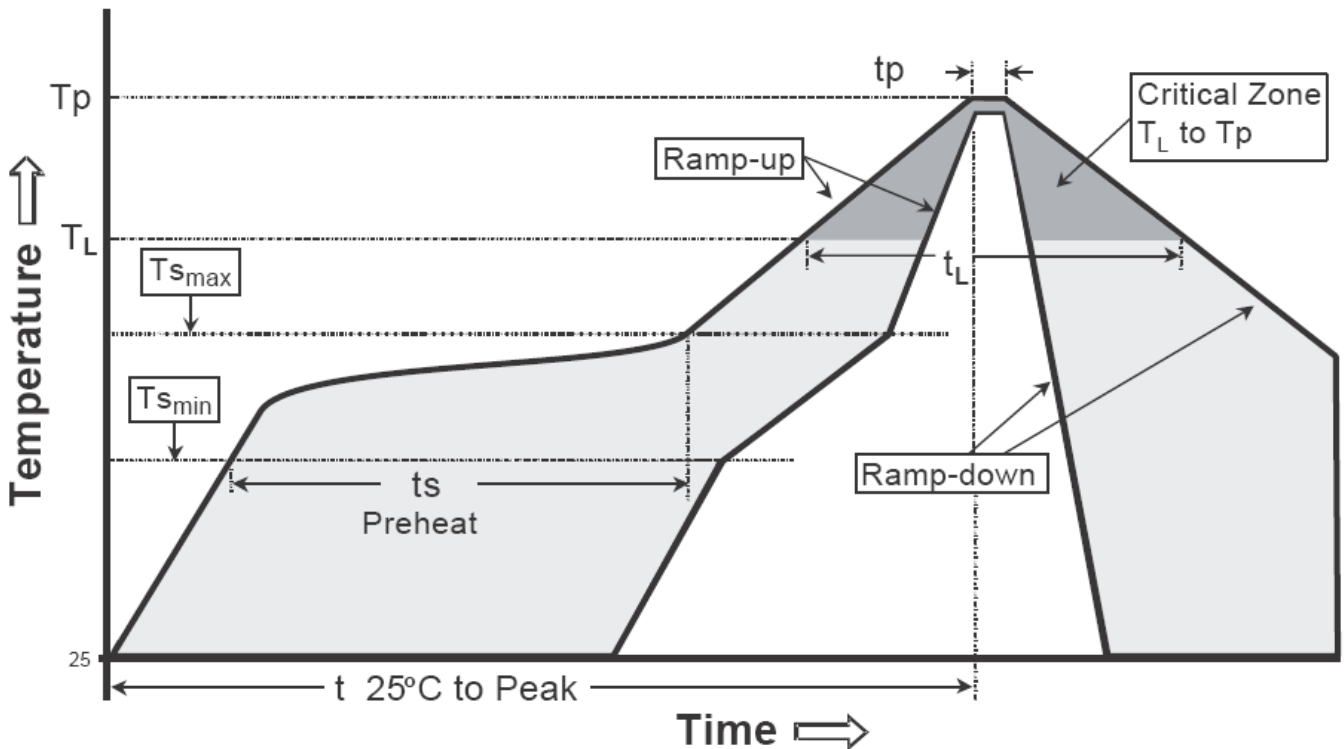
Carrier Tape Dimension



Recommended wave soldering condition

| | | |
|-----------------|------------------|-----------------|
| Product | Peak Temperature | Soldering Time |
| Pb-free devices | 260 +0/-5 °C | 5 +1/-1 seconds |

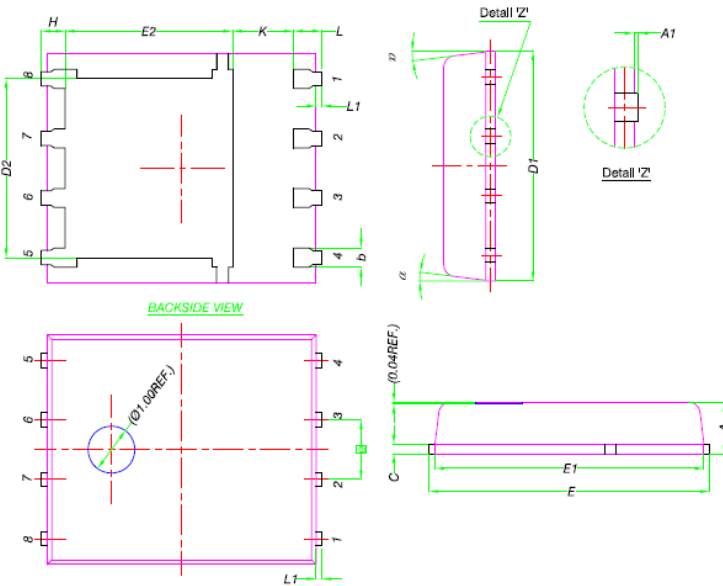
Recommended temperature profile for IR reflow



| Profile feature | Sn-Pb eutectic Assembly | Pb-free Assembly |
|-------------------------------------------------------------|-------------------------|------------------|
| Average ramp-up rate (T _{smax} to T _p) | 3°C/second max. | 3°C/second max. |
| Preheat | | |
| -Temperature Min(T _{s min}) | 100°C | 150°C |
| -Temperature Max(T _{s max}) | 150°C | 200°C |
| -Time(t _{s min} to t _{s max}) | 60-120 seconds | 60-180 seconds |
| Time maintained above: | | |
| -Temperature (T _L) | 183°C | 217°C |
| - Time (t _L) | 60-150 seconds | 60-150 seconds |
| Peak Temperature(T _p) | 240 +0/-5 °C | 260 +0/-5 °C |
| Time within 5°C of actual peak temperature(tp) | 10-30 seconds | 20-40 seconds |
| Ramp down rate | 6°C/second max. | 6°C/second max. |
| Time 25 °C to peak temperature | 6 minutes max. | 8 minutes max. |

Note :1. All temperatures refer to topside of the package, measured on the package body surface.
 2. For devices mounted on FR-4 PCB of 1.6mm or equivalent grade PCB. If other grade PCB is used, care should be taken to match the coefficients of thermal expansion between components and PCB. If they are not matched well, the solder joints may crack or the bodies of the parts may crack or shatter as the assembly cools.

DFN5x6 Dimension



Marking:

Device Name →

B3D0

N03B

Date Code →

Date Code :

1st digit : year code, last digit of Christian year

2nd digit : month code, Jan→A, Feb→B, Mar→C, Apr→D, May→E, Jun→F, Jul→G, Aug→H, Sep→J, Oct→K, Nov→L, Dec→M

3rd and 4th digits : serial number of production lot

8-Lead DFN5x6 Plastic Package
 CYS Package Code : H8

| DIM | Millimeters | | Inches | | DIM | Millimeters | | Inches | |
|-----|-------------|------|--------|-------|-----|-------------|------|--------|-------|
| | Min. | Max. | Min. | Max. | | Min. | Max. | Min. | Max. |
| A | 0.90 | 1.10 | 0.035 | 0.043 | E2 | 3.38 | 3.78 | 0.133 | 0.149 |
| A1 | 0.00 | 0.05 | 0.000 | 0.002 | e | 1.27 | BSC | 0.050 | BSC |
| b | 0.33 | 0.51 | 0.013 | 0.020 | H | 0.41 | 0.61 | 0.016 | 0.024 |
| C | 0.20 | 0.30 | 0.008 | 0.012 | K | 1.10 | - | 0.043 | - |
| D1 | 4.80 | 5.00 | 0.189 | 0.197 | L | 0.51 | 0.71 | 0.020 | 0.028 |
| D2 | 3.61 | 3.96 | 0.142 | 0.156 | L1 | 0.06 | 0.20 | 0.002 | 0.008 |
| E | 5.90 | 6.10 | 0.232 | 0.240 | θ | 8° | 12° | 8° | 12° |
| E1 | 5.70 | 5.80 | 0.224 | 0.228 | | | | | |

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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