

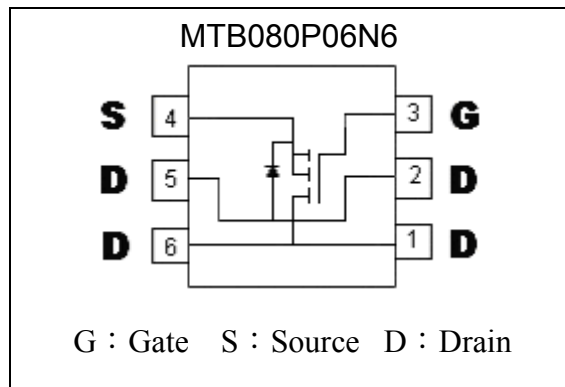
P-Channel Enhancement Mode Power MOSFET

MTB080P06N6

BV_{DSS}		-60V
$I_D@V_{GS}=-4.5V, T_C=25^\circ C$		-3.8A
$I_D@V_{GS}=-4.5V, T_A=25^\circ C$		-3.0A
$R_{DSON(TYP)}$	$V_{GS}=-10V, I_D=-3A$	79m Ω
	$V_{GS}=-4.5V, I_D=-2.7A$	107m Ω

Features

- Simple drive requirement
- Low on-resistance
- Small package outline
- Pb-free lead plating and halogen-free package

Equivalent Circuit

Absolute Maximum Ratings ($T_a=25^\circ C$)

Parameter		Symbol	Limits	Unit
Drain-Source Voltage		V_{DS}	-60	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	$T_C=25^\circ C, V_{GS}=-10V$	I_D	-3.8	A
	$T_C=70^\circ C, V_{GS}=-10V$		-3.0	
	$T_A=25^\circ C, V_{GS}=-10V$ (Note 1)		-3.0	
	$T_A=70^\circ C, V_{GS}=-10V$ (Note 1)		-2.4	
Pulsed Drain Current (Note 2, 3)		I_{DM}	-40	
Total Power Dissipation	$T_C=25^\circ C$	P_D	3.1	W
	$T_C=70^\circ C$		2.0	
	$T_A=25^\circ C$ (Note 1)		2.0	
	$T_A=70^\circ C$ (Note 1)		1.25	
Operating Junction Temperature and Storage Temperature Range		T_j, T_{stg}	-55~+150	$^\circ C$

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	$R_{th,j-c}$	40	$^\circ C/W$
Thermal Resistance, Junction-to-ambient, max (Note 1)	$R_{\theta JA}$	62.5	

 Note : 1.Surface mounted on 1 in² copper pad of FR-4 board, $t \leq 5$ sec. 156 $^\circ C/W$ when mounted on minimum copper pad.

2.Pulse width limited by maximum junction temperature.

 3.Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$



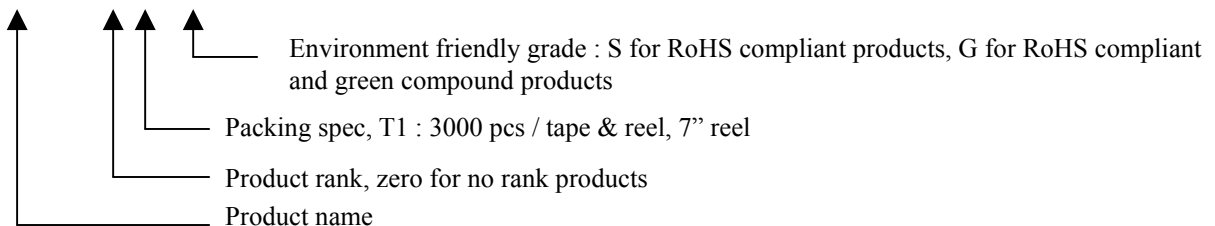
Electrical Characteristics (Ta=25°C, unless otherwise noted)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	-60	-	-	V	V _{GS} =0V, I _D =-250μA
ΔBV _{DSS} /ΔT _j	-	-56	-	mV/°C	Reference to 25°C, I _D =-250μA
V _{GS(th)}	-1	-	-2.5	V	V _{DS} =V _{GS} , I _D =-250μA
I _{GSS}	-	-	±100	nA	V _{GS} =±20V, V _{DS} =0V
I _{DSS}	-	-	-1	μA	V _{DS} =-60V, V _{GS} =0V, T _j =25°C
	-	-	-10		V _{DS} =-48V, V _{GS} =0V, T _j =55°C
*R _{DSON}	-	79	104	mΩ	I _D =-3A, V _{GS} =-10V
	-	107	150		I _D =-2.7A, V _{GS} =-4.5V
*G _{FS}	-	6.1	-	S	V _{DS} =-10V, I _D =-3A
Dynamic					
C _{iSS}	-	512	-	pF	V _{DS} =-25V, V _{GS} =0V, f=1MHz
C _{oSS}	-	58	-		
C _{rSS}	-	40	-		
t _{d(ON)}	-	6.4	-	ns	V _{DS} =-30V, I _D =-3A, V _{GS} =-10V, R _G =3Ω
t _r	-	16.6	-		
t _{d(OFF)}	-	25.8	-		
t _f	-	7.4	-		
Q _g	-	12	-	nC	V _{DS} =-10V, I _D =-3A, V _{GS} =-10V
Q _{gs}	-	1.7	-		
Q _{gd}	-	3.0	-		
Source-Drain Diode					
*I _S	-	-	-3	A	
*I _{SM}	-	-	-15		
*V _{SD}	-	-0.82	-1.2	V	I _S =-2A, V _{GS} =0V
*T _{rr}	-	11.1	-	ns	I _F =-3A, V _{GS} =0V, dI _F /dt=100A/μs
Q _{rr}	-	7.3	-	nC	

*Pulse Test : Pulse Width ≤300μs, Duty Cycle ≤2%

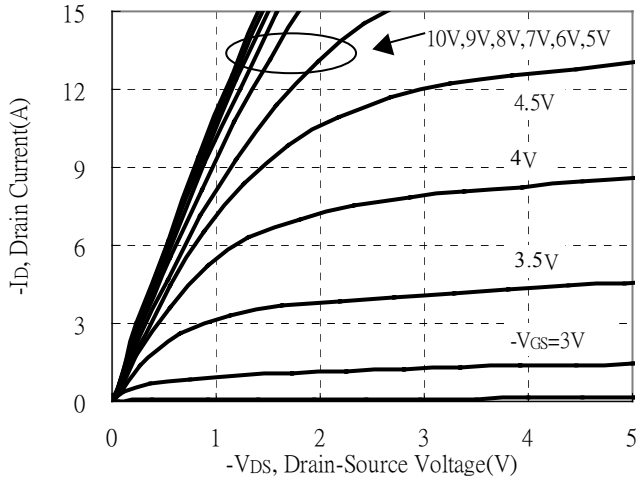
Ordering Information

Device	Package	Shipping
MTB080P06N6-0-T1-G	SOT-26 (Pb-free lead plating and halogen-free package)	3000 pcs / Tape & Reel

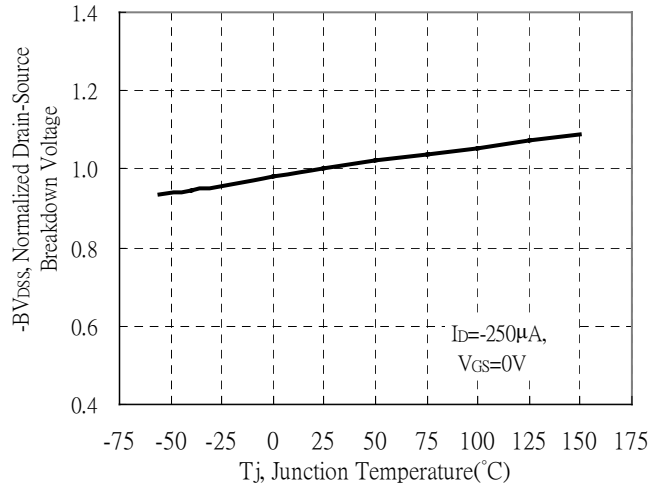


Typical Characteristics

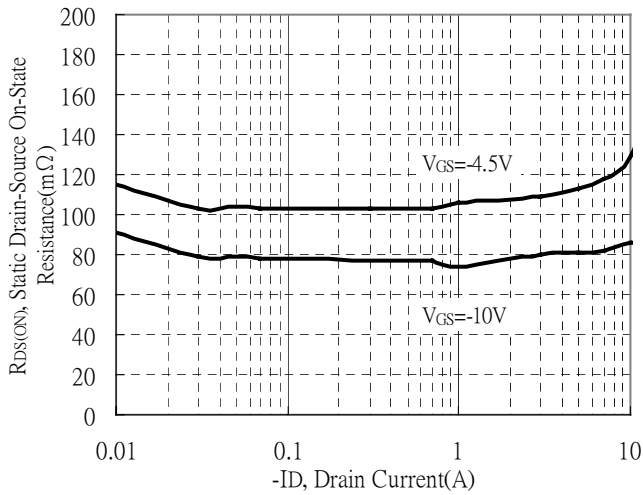
Typical Output Characteristics



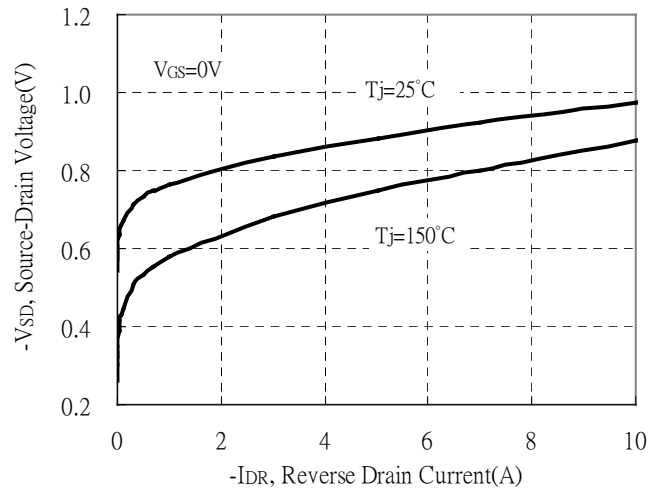
Brekdown Voltage vs Ambient Temperature



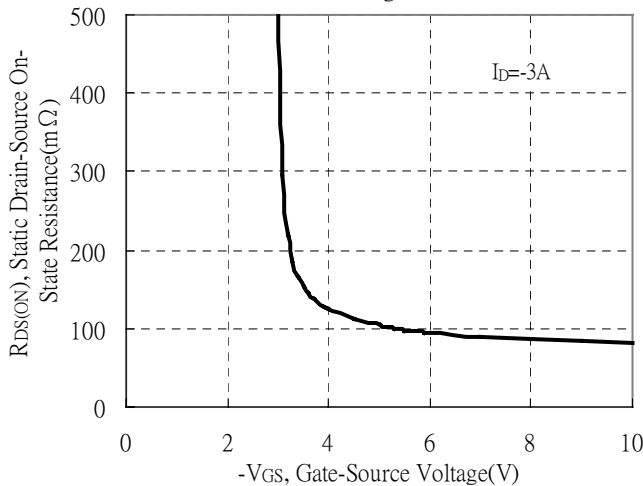
Static Drain-Source On-State resistance vs Drain Current



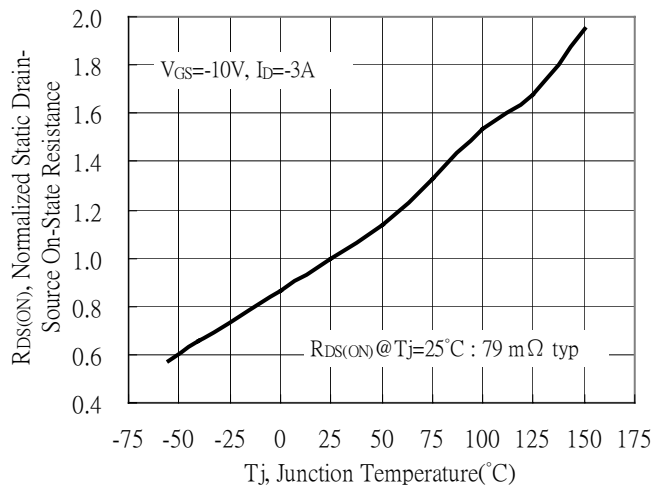
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

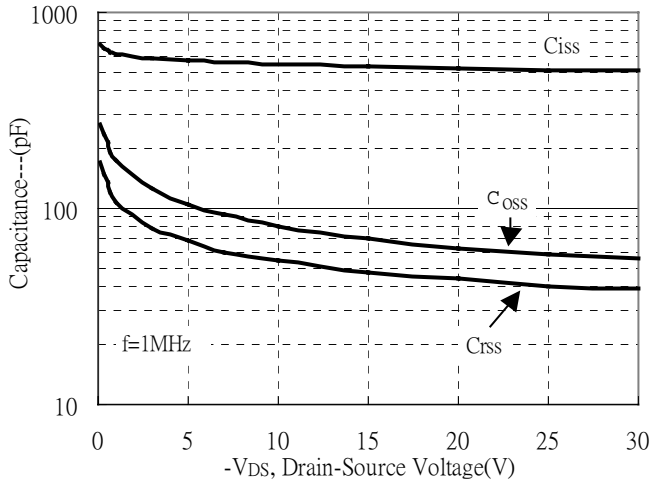


Drain-Source On-State Resistance vs Junction Temperature

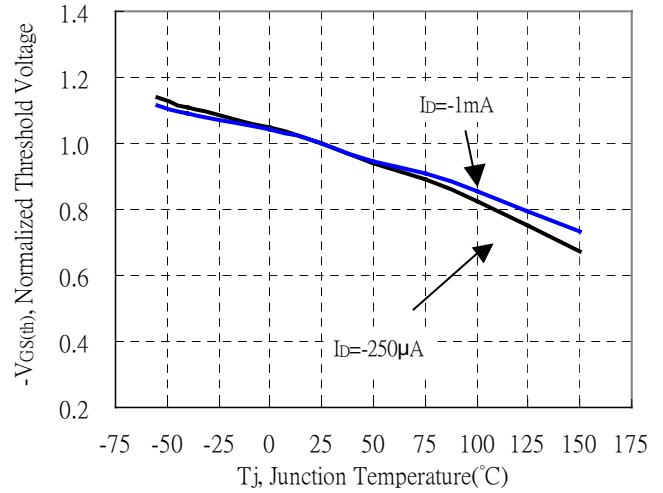


Typical Characteristics(Cont.)

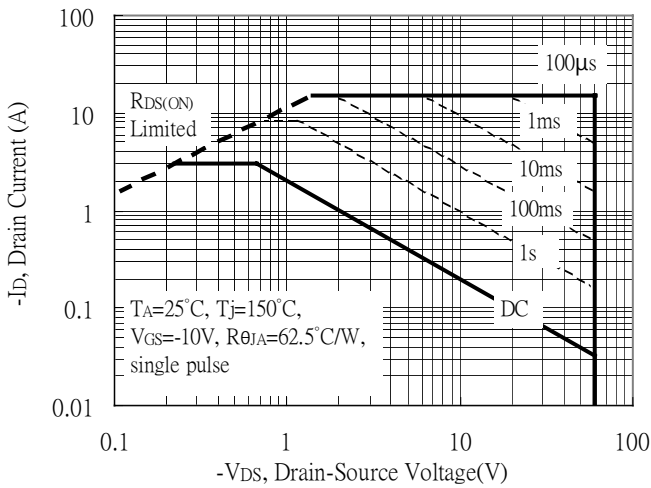
Capacitance vs Drain-to-Source Voltage



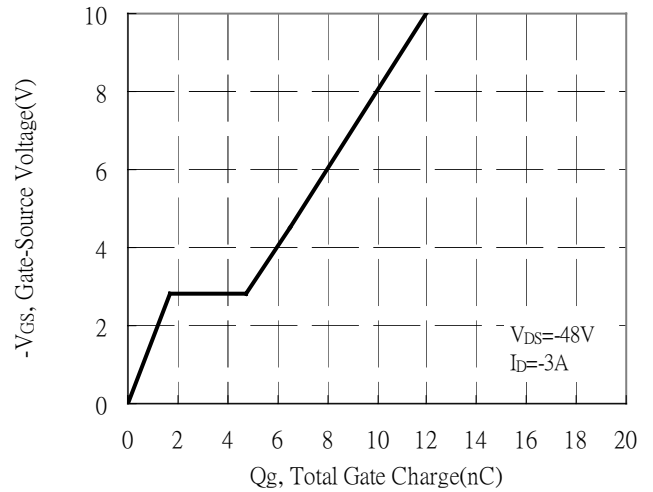
Threshold Voltage vs Junction Temperature



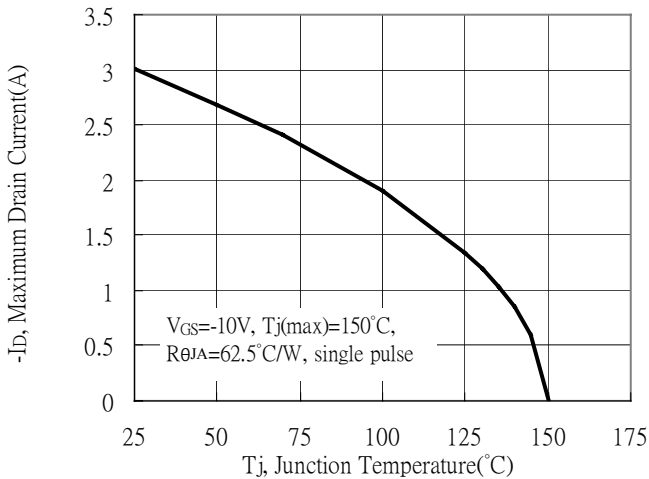
Maximum Safe Operating Area



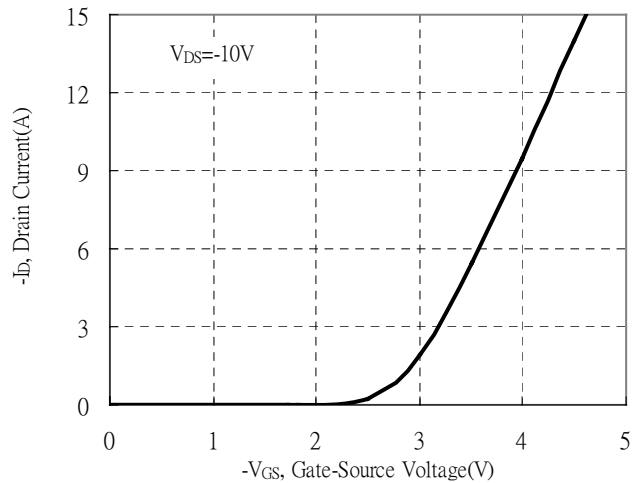
Gate Charge Characteristics



Maximum Drain Current vs Junction Temperature

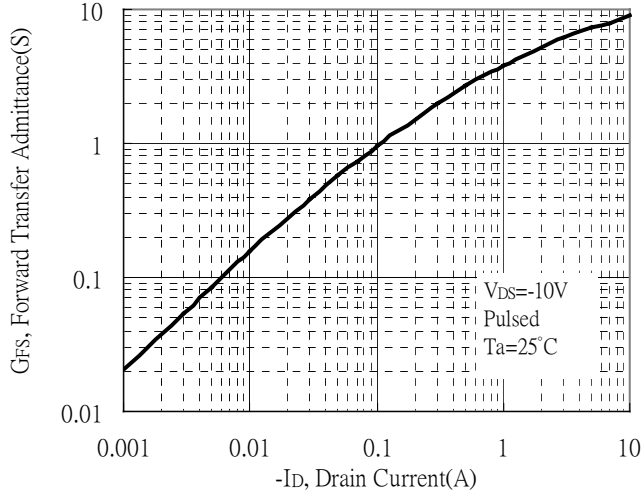


Typical Transfer Characteristics

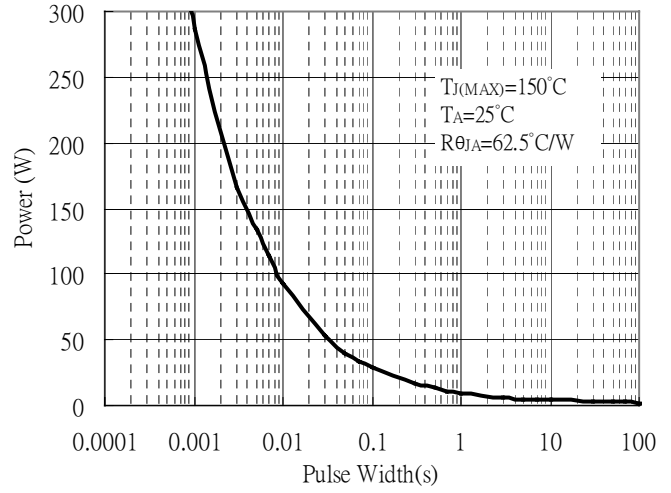


Typical Characteristics(Cont.)

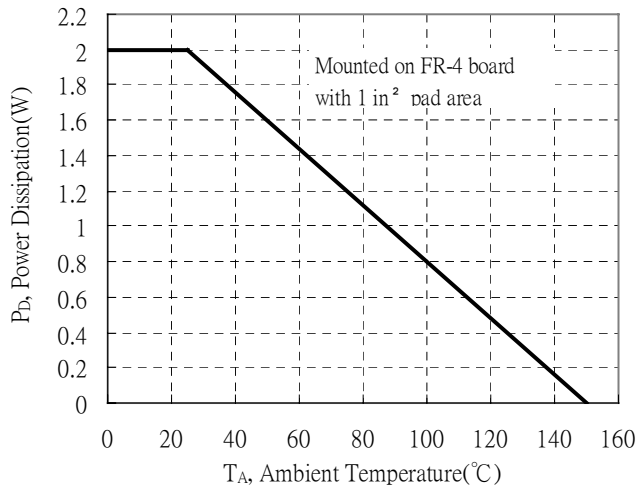
Forward Transfer Admittance vs Drain Current



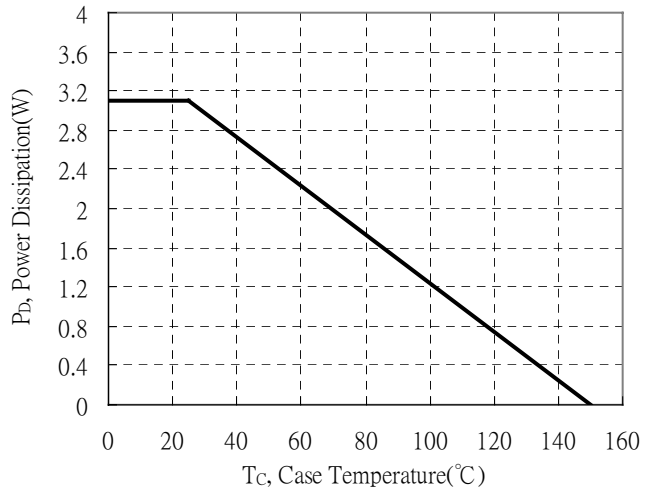
Single Pulse Power Rating, Junction to Case



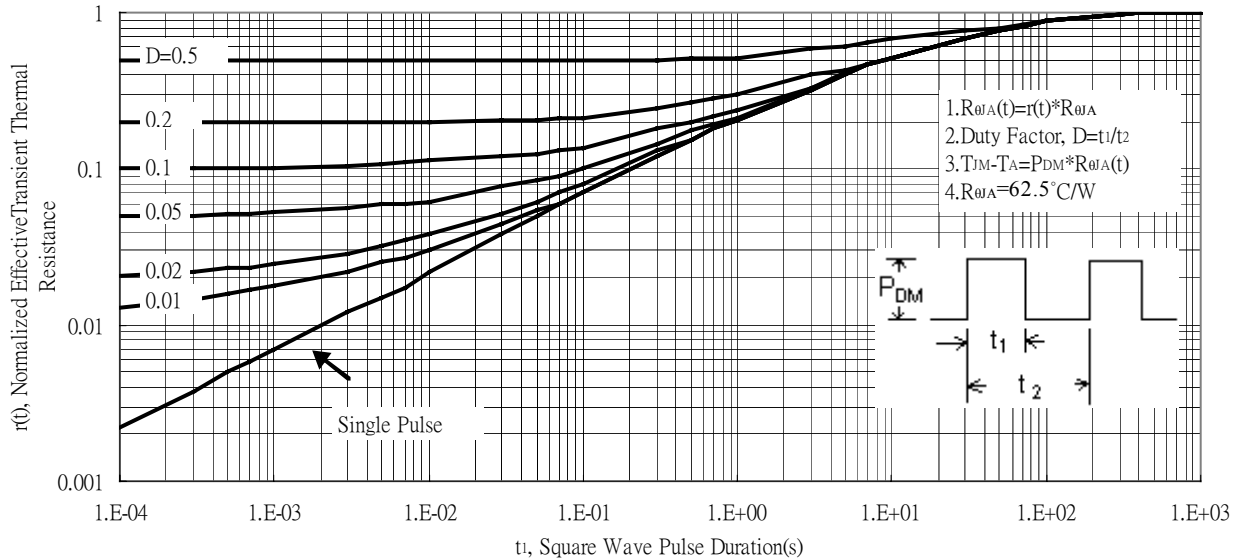
Power Derating Curve



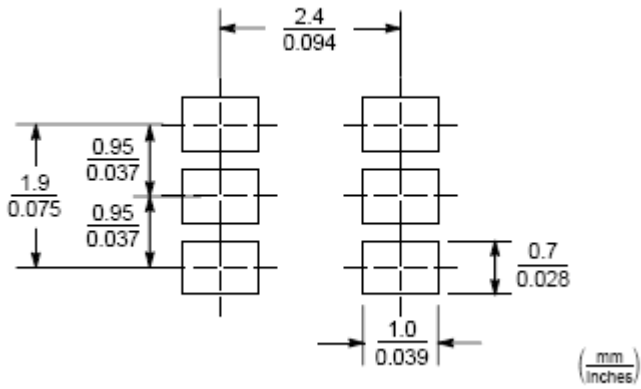
Power Derating Curve



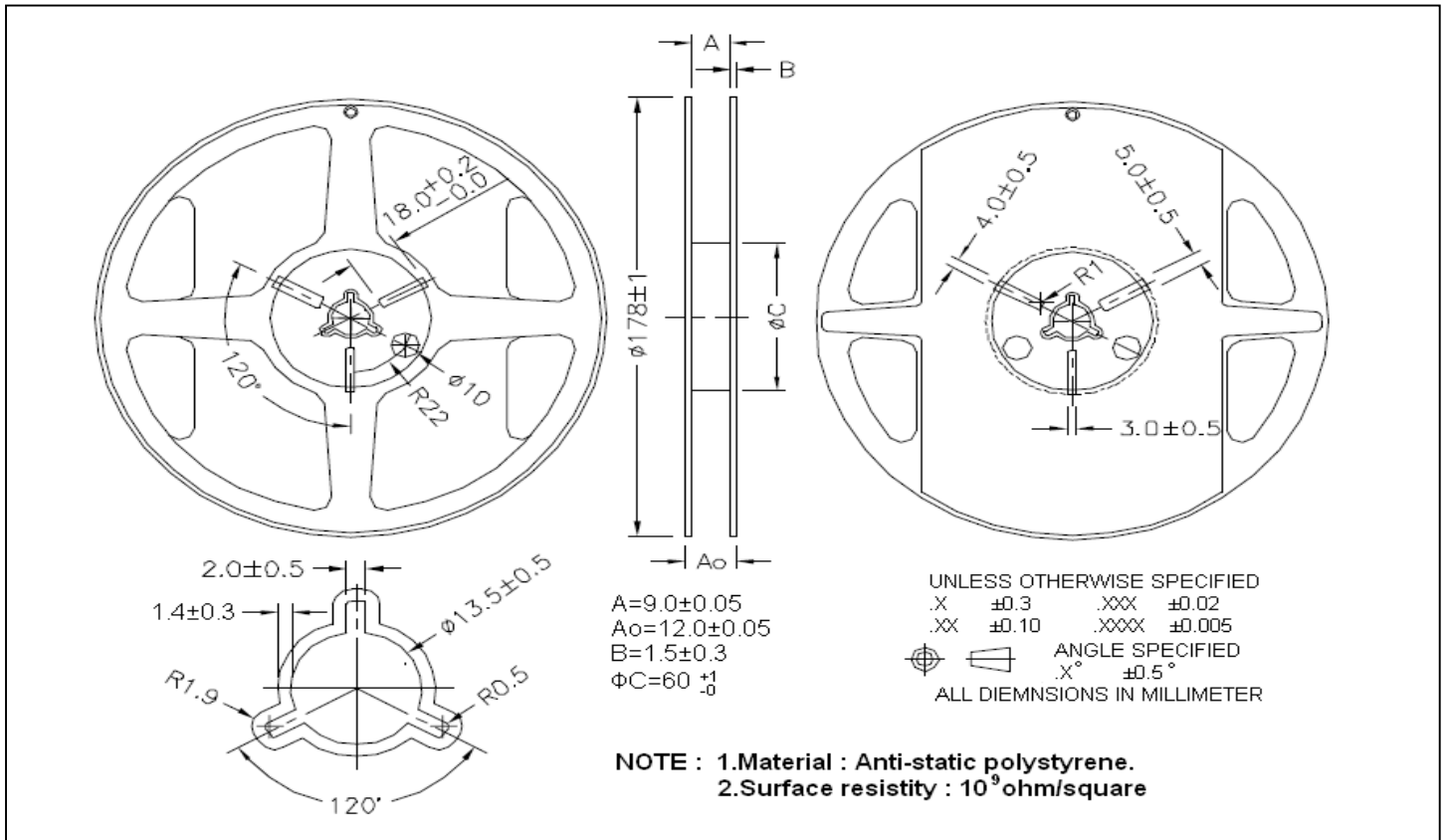
Transient Thermal Response Curves



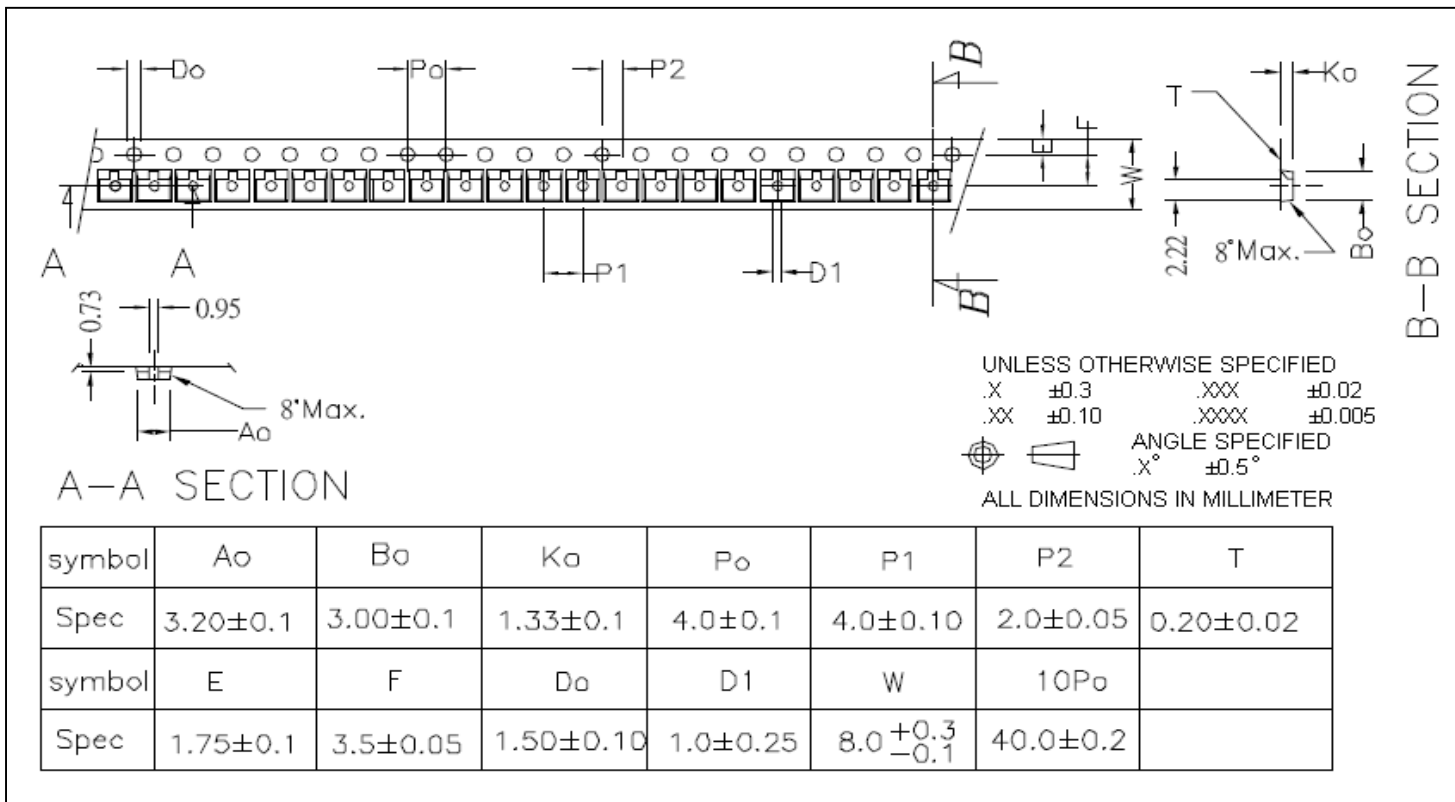
Recommended Soldering Footprint



Reel Dimension

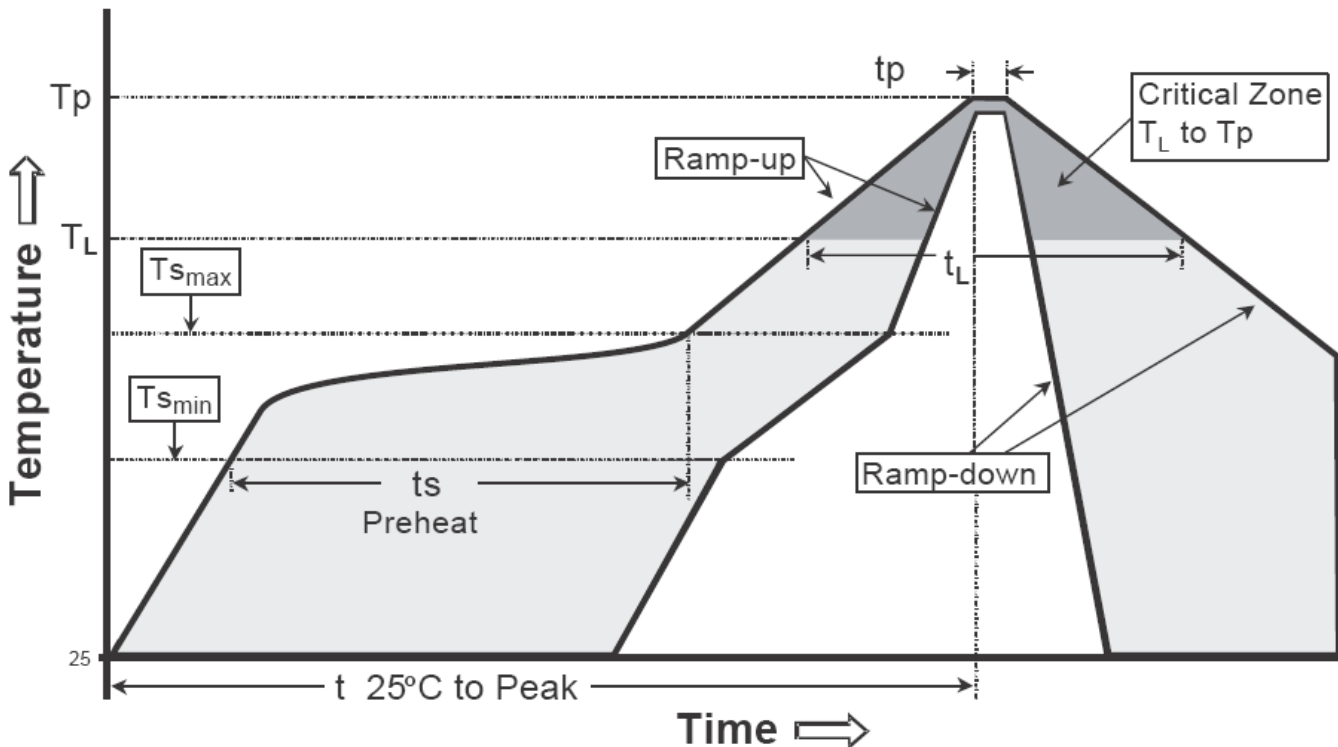


Carrier Tape Dimension



Recommended wave soldering condition

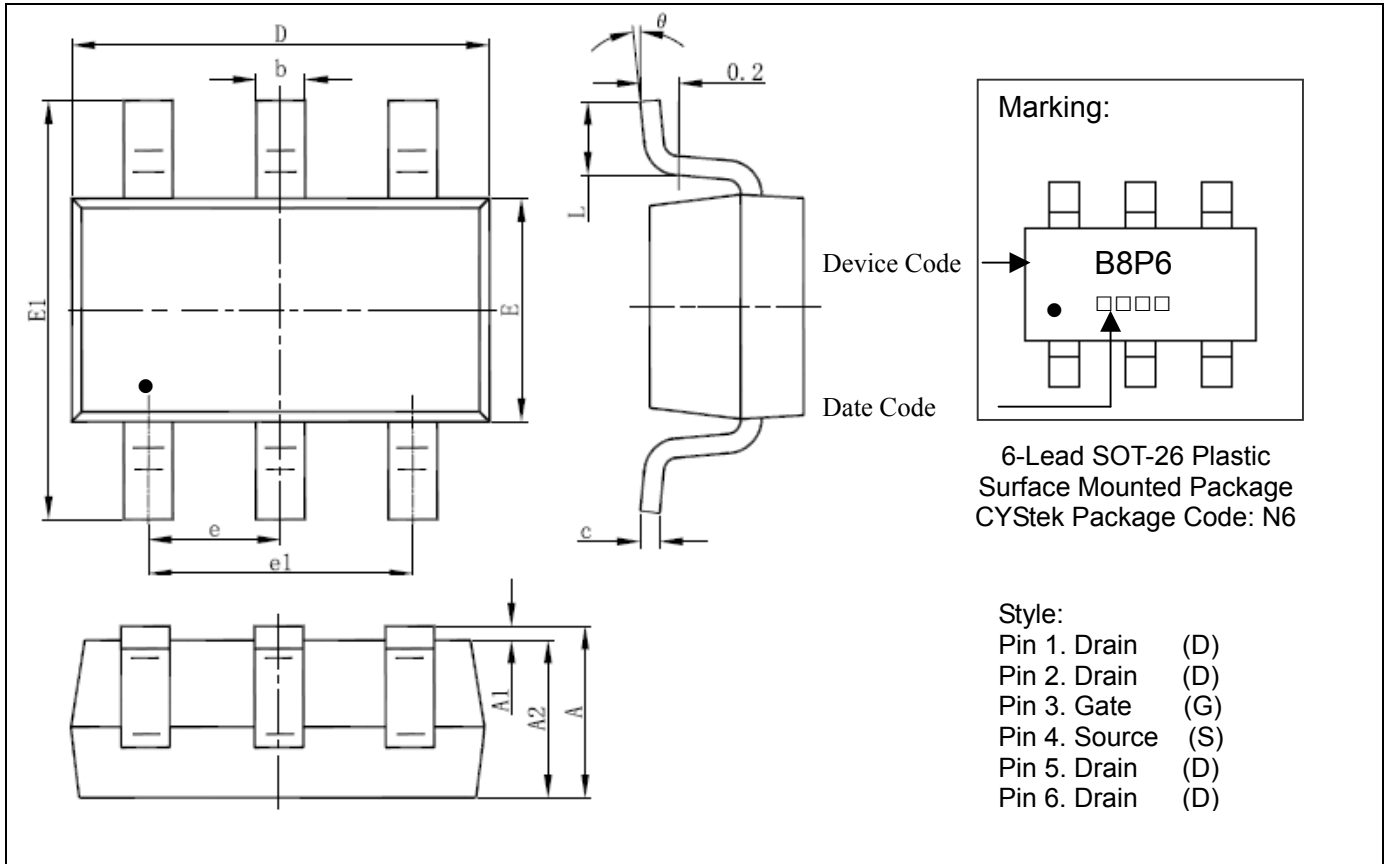
Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

Recommended temperature profile for IR reflow


Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _p)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

SOT-26 Dimension



DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049	E	1.500	1.700	0.059	0.067
A1	0.000	0.100	0.000	0.004	E1	2.650	2.950	0.104	0.116
A2	1.050	1.150	0.041	0.045	e	0.950 (BSC)		0.037 (BSC)	
b	0.300	0.500	0.012	0.020	e1	1.800	2.000	0.071	0.079
c	0.100	0.200	0.004	0.008	L	0.300	0.600	0.012	0.024
D	2.820	3.020	0.111	0.119	θ	0°	8°	0°	8°

Notes : 1. Controlling dimension : millimeters.
 2. Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3. If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material :

- Lead : Pure tin plated.
- Mold Compound : Epoxy resin family, flammability solid burning class:UL94V-0.

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