

N-Channel Enhancement Mode Power MOSFET

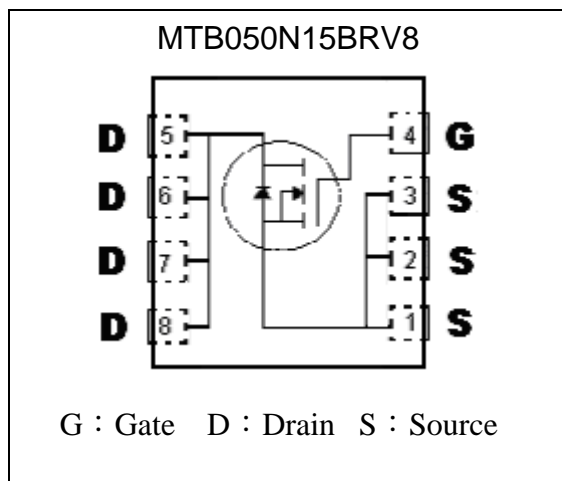
MTB050N15BRV8

BV_{DSS}		150V
I_D @ $T_C=25^\circ\text{C}$, $V_{GS}=10\text{V}$		12.4A
I_D @ $T_A=25^\circ\text{C}$, $V_{GS}=10\text{V}$		4.3A
$R_{DSON(TYP)}$	$V_{GS}=10\text{V}$, $I_D=3.4\text{A}$	47.5m Ω
	$V_{GS}=4.5\text{V}$, $I_D=3.3\text{A}$	53m Ω

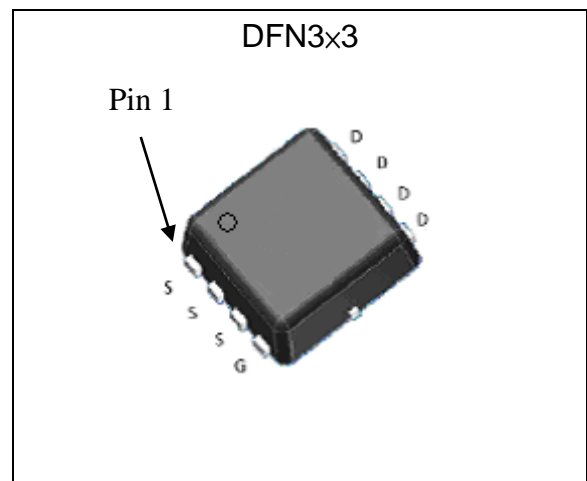
Features

- Single Drive Requirement
- Low On-resistance
- Fast Switching Characteristic
- Pb-free lead plating and halogen-free package

Equivalent Circuit

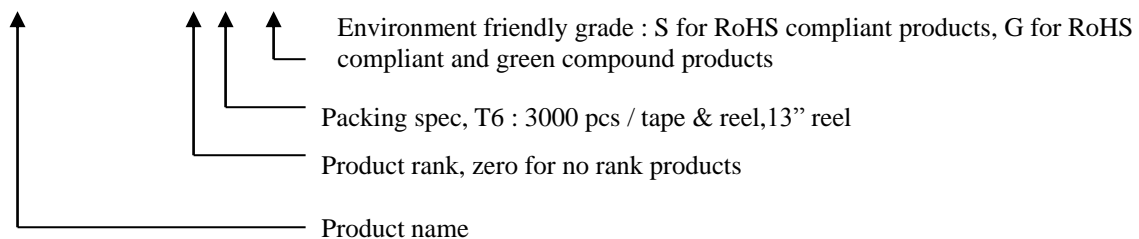


Outline



Ordering Information

Device	Package	Shipping
MTB050N15BRV8-0-T6-G	DFN3x3 (Pb-free lead plating and halogen-free package)	3000 pcs / Tape & Reel





Absolute Maximum Ratings (Ta=25°C, unless otherwise specified)

Parameter	Symbol	Limits	Unit	
Drain-Source Voltage	V _{DS}	150	V	
Gate-Source Voltage	V _{GS}	±20		
Continuous Drain Current @ V _{GS} =10V, T _C =25°C	I _D	12.4	A	
Continuous Drain Current @ V _{GS} =10V, T _C =100°C		7.8		
Continuous Drain Current @ V _{GS} =10V, T _A =25°C	I _{DSM}	4.3		
Continuous Drain Current @ V _{GS} =10V, T _A =70°C		3.4		
Pulsed Drain Current	I _{DM}	50 *1		
Avalanche Current @ L=0.1mH	I _{AS}	36		
Avalanche Energy @ L=1mH, I _D =16A, V _{DD} =25V	E _{AS}	128	mJ	
Total Power Dissipation	P _D	T _C =25°C	21	W
		T _C =100°C	8.4	
	P _{DSM}	T _A =25°C	2.5 *2	
		T _A =70°C	1.6 *2	
Operating Junction and Storage Temperature Range	T _j , T _{stg}	-55~+150	°C	

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	R _{θJC}	6	°C/W
Thermal Resistance, Junction-to-ambient, max	R _{θJA}	50 *2	

- Note : 1. Pulse width limited by maximum junction temperature.
 2. Surface mounted on a 1 in² pad of 2oz copper, t≤10s. In practice R_{θJA} will be determined by customer's PCB characteristics. 125°C/W when mounted on a minimum pad of 2 oz. copper.
 3. 100% tested by conditions of L=0.1mH, I_{AS}=4.5A, V_{GS}=10V, V_{DD}=25V

Characteristics (Tc=25°C, unless otherwise specified)

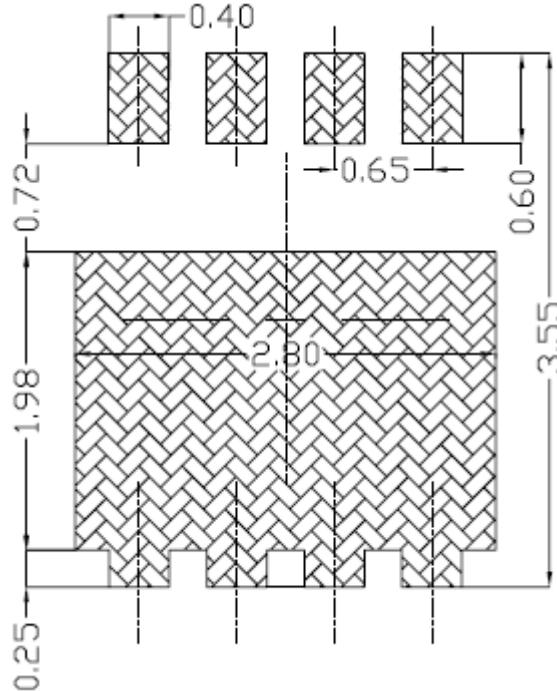
Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	150	-	-	V	V _{GS} =0V, I _D =250μA
V _{GS(th)}	1	-	2.5		V _{DS} = V _{GS} , I _D =250μA
G _{FS} *1	-	15.3	-	S	V _{DS} =5V, I _D =5A
I _{GSS}	-	-	±100	nA	V _{GS} =±20V, V _{DS} =0V
I _{DSS}	-	-	1	μA	V _{DS} =120V, V _{GS} =0V
	-	-	5		V _{DS} =120V, V _{GS} =0V, T _j =55°C
R _{DS(ON)} *1	-	47.5	65	mΩ	V _{GS} =10V, I _D =3.4A
	-	53.0	76		V _{GS} =4.5V, I _D =3.3A
Dynamic					
C _{iss}	-	1385	-	pF	V _{DS} =80V, V _{GS} =0V, f=1MHz
C _{oss}	-	65	-		
C _{rss}	-	23	-		
Q _g *1, 2	-	25.4	-	nC	V _{DS} =120V, V _{GS} =10V, I _D =5.4A
Q _{gs} *1, 2	-	4.3	-		
Q _{gd} *1, 2	-	5.3	-		

Characteristics (Tc=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
t _{d(ON)} *1, 2	-	13.2	-	ns	V _{DS} =50V, I _D =1A, V _{GS} =10V, R _{GS} =6Ω
t _r *1, 2	-	17.2	-		
t _{d(OFF)} *1, 2	-	47	-		
t _f *1, 2	-	24.2	-		
R _g	-	1	-	Ω	f=1MHz
Source-Drain Diode					
I _S *1	-	-	16	A	
V _{SD} *1	-	0.78	1.2	V	I _S =3.2A, V _{GS} =0V
t _{rr}	-	43.3	-	ns	I _F =3.2A, dI _F /dt=100A/μs
Q _{rr}	-	68.6	-	nC	

Note : *1.Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%
 *2.Independent of operating temperature

Recommended Soldering Footprint

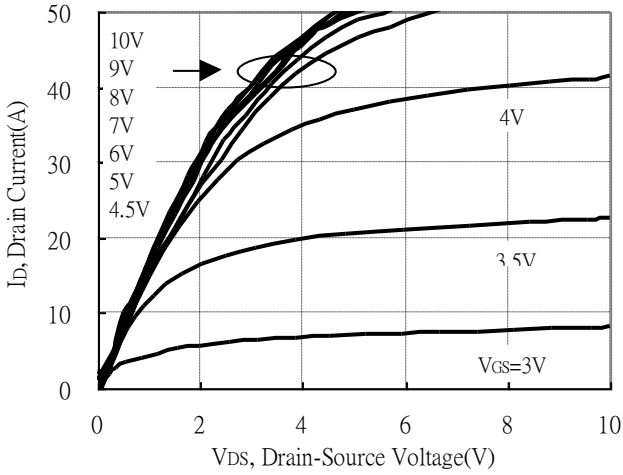


unit : mm

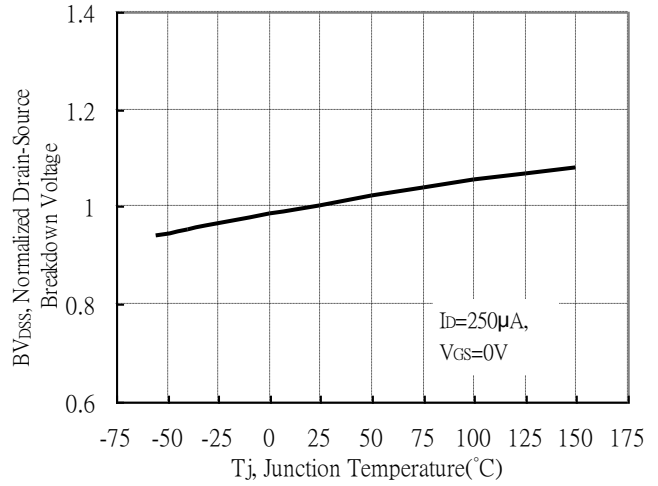


Typical Characteristics

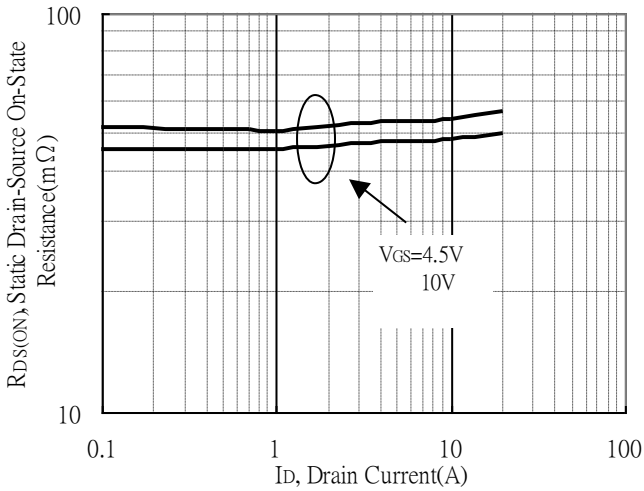
Typical Output Characteristics



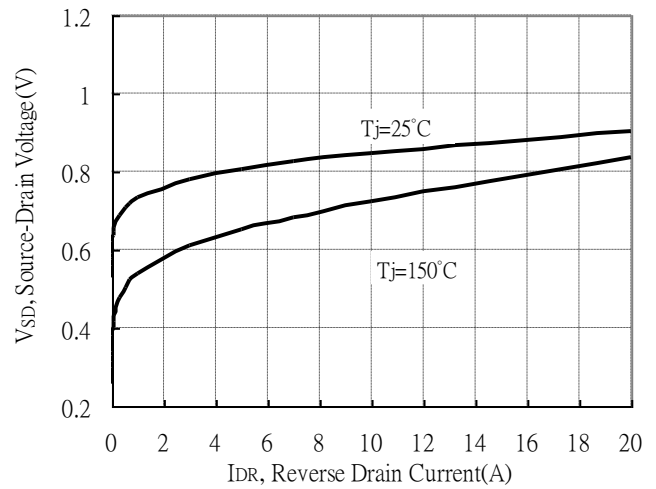
Brekdown Voltage vs Ambient Temperature



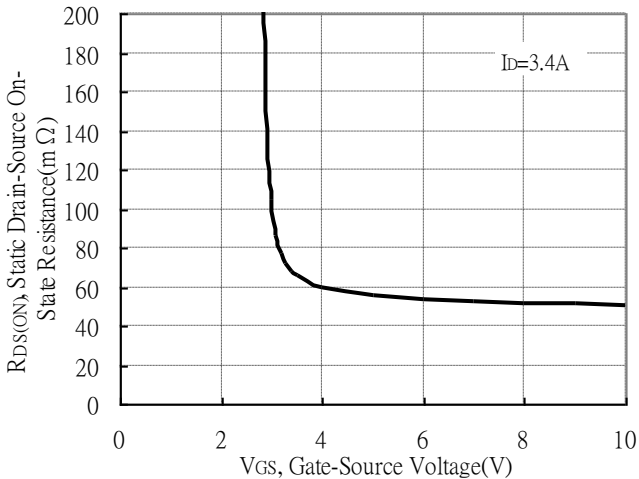
Static Drain-Source On-State resistance vs Drain Current



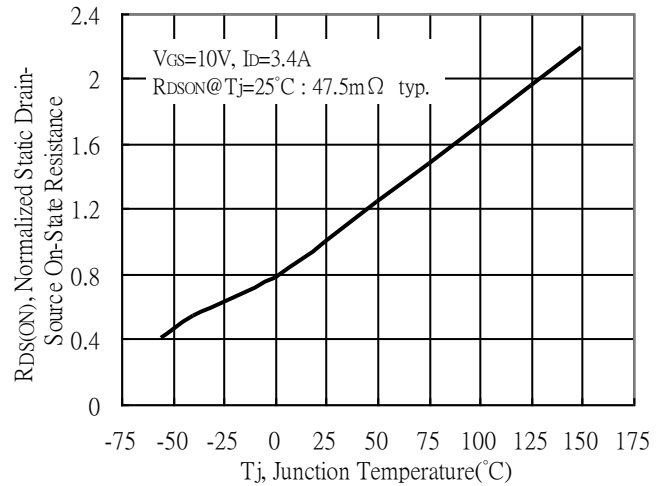
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

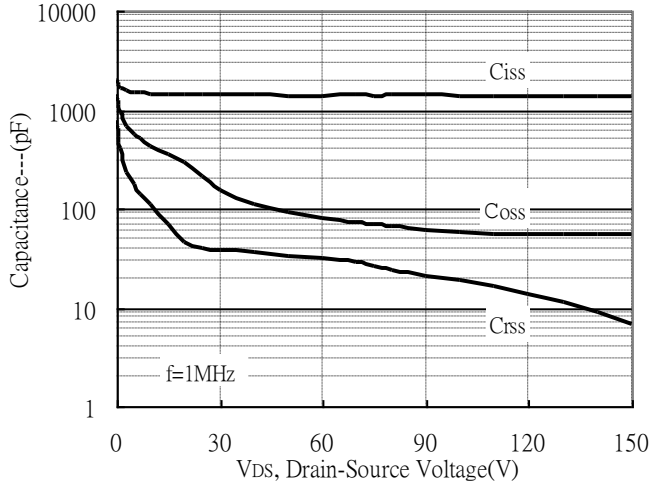


Drain-Source On-State Resistance vs Junction Temperature

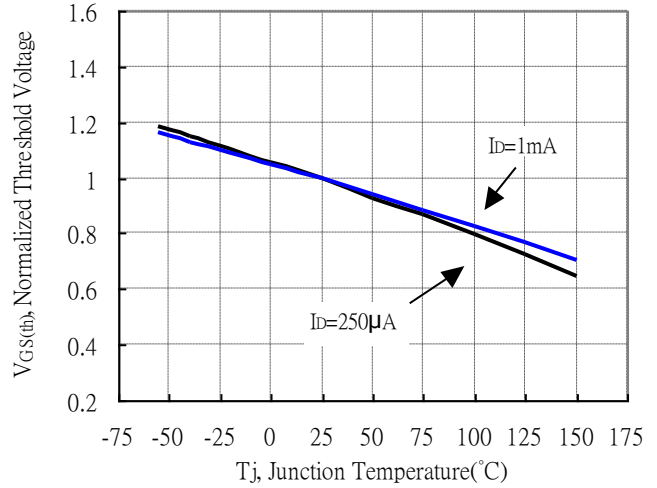


Typical Characteristics(Cont.)

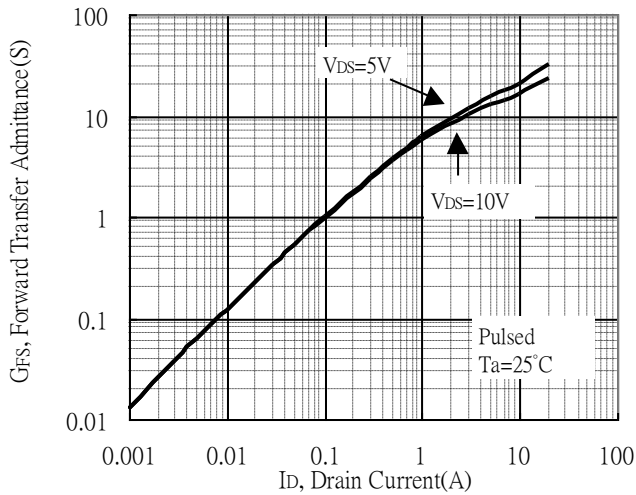
Capacitance vs Drain-to-Source Voltage



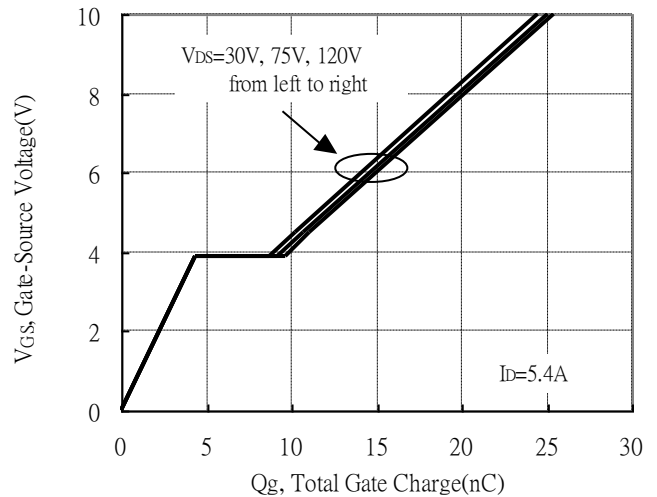
Threshold Voltage vs Junction Temperature



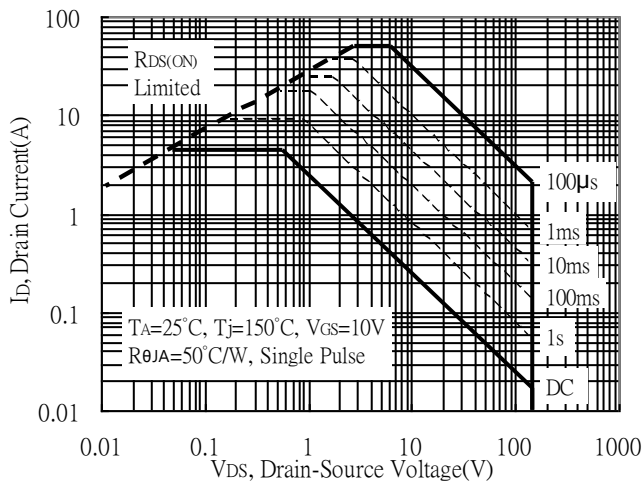
Forward Transfer Admittance vs Drain Current



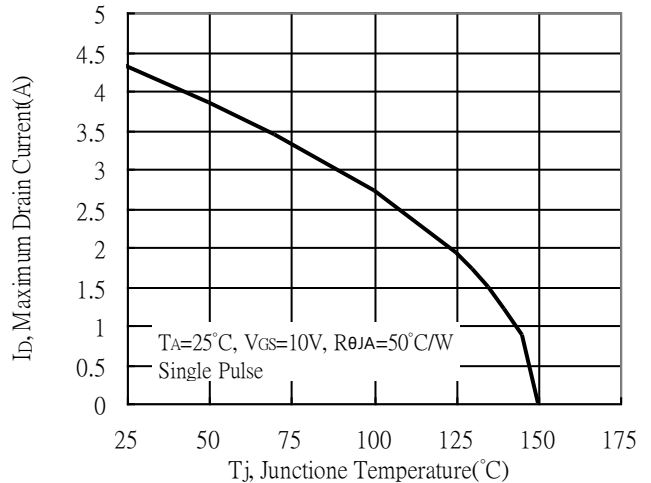
Gate Charge Characteristics



Maximum Safe Operating Area



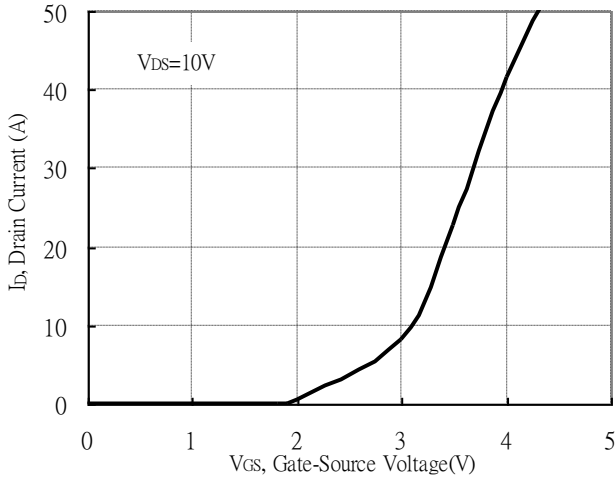
Maximum Drain Current vs Junction Temperature



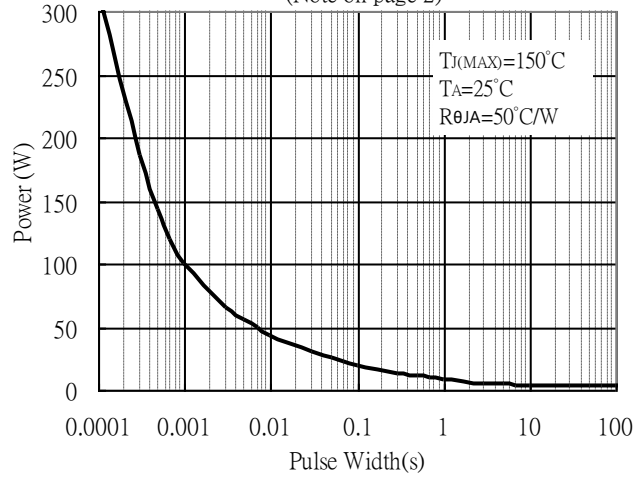


Typical Characteristics(Cont.)

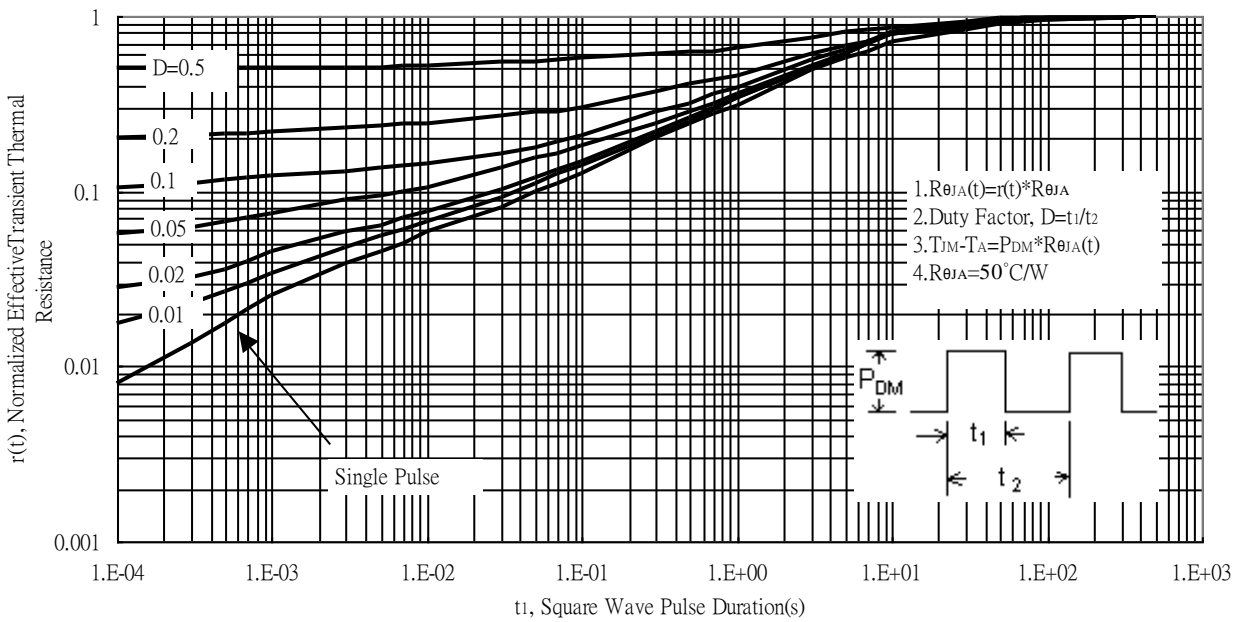
Typical Transfer Characteristics



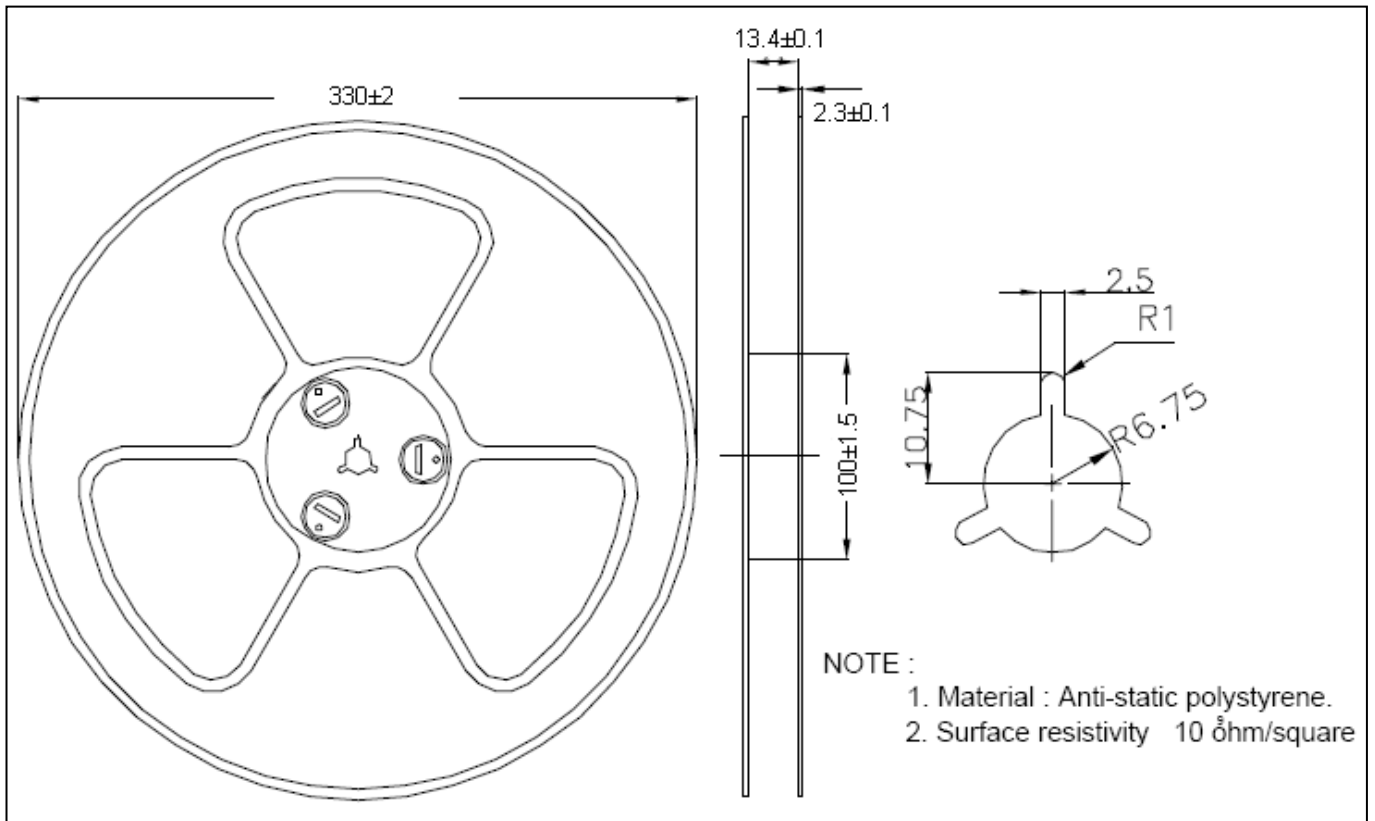
Single Pulse Power Rating, Junction to Ambient
 (Note on page 2)



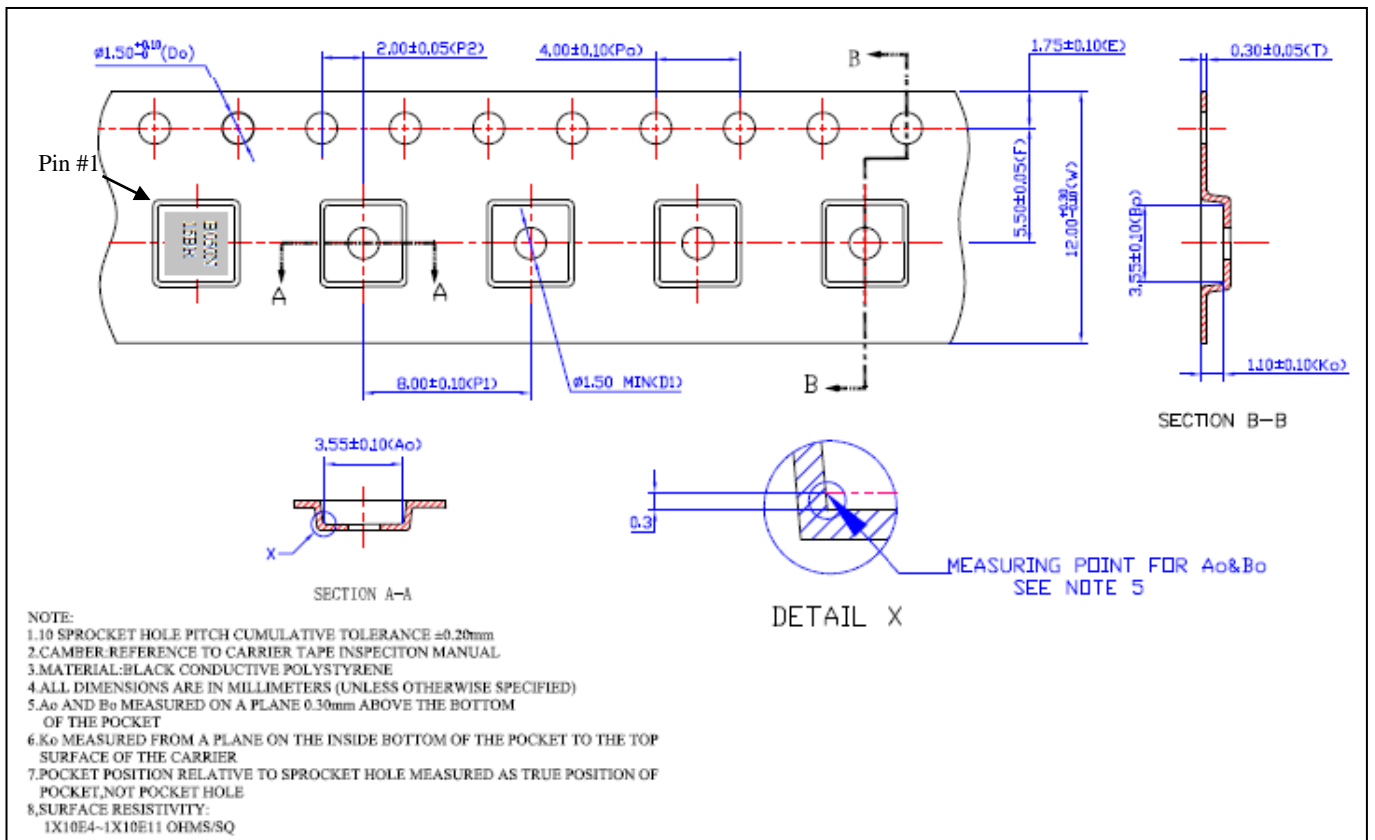
Transient Thermal Response Curves



Reel Dimension



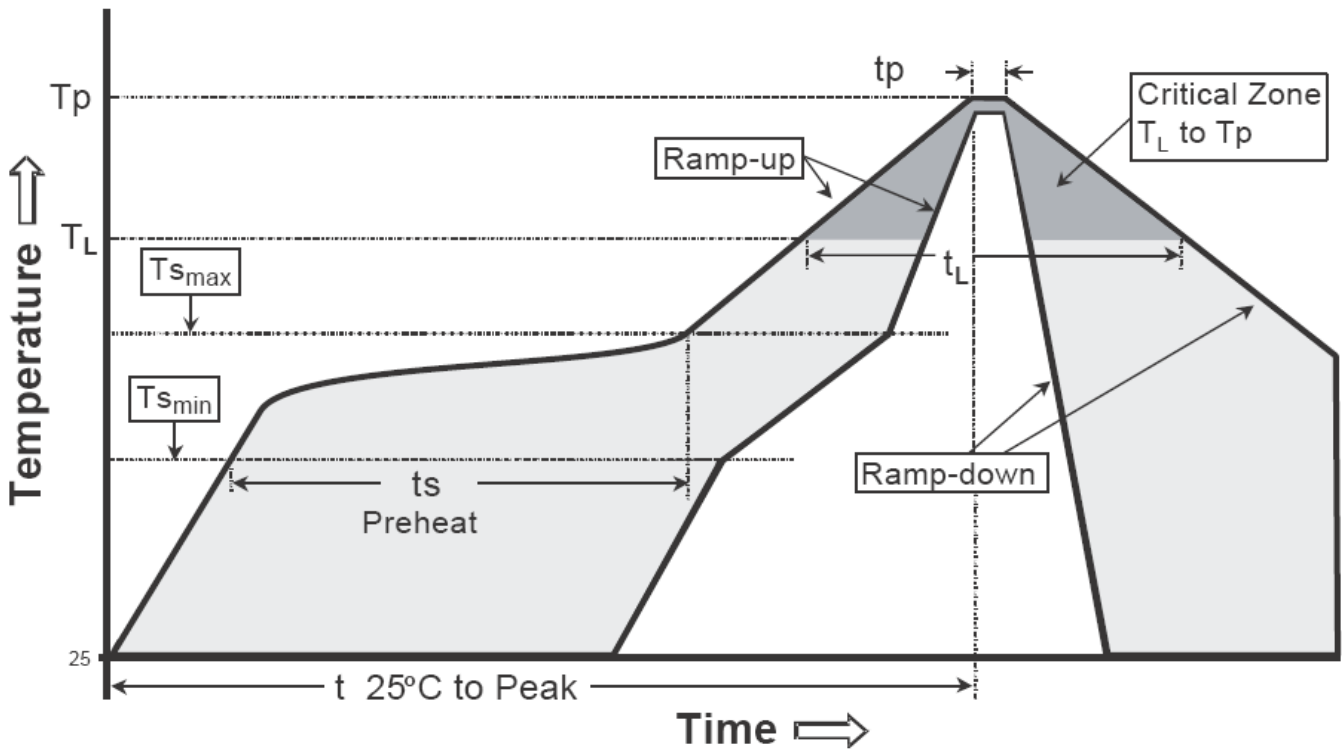
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

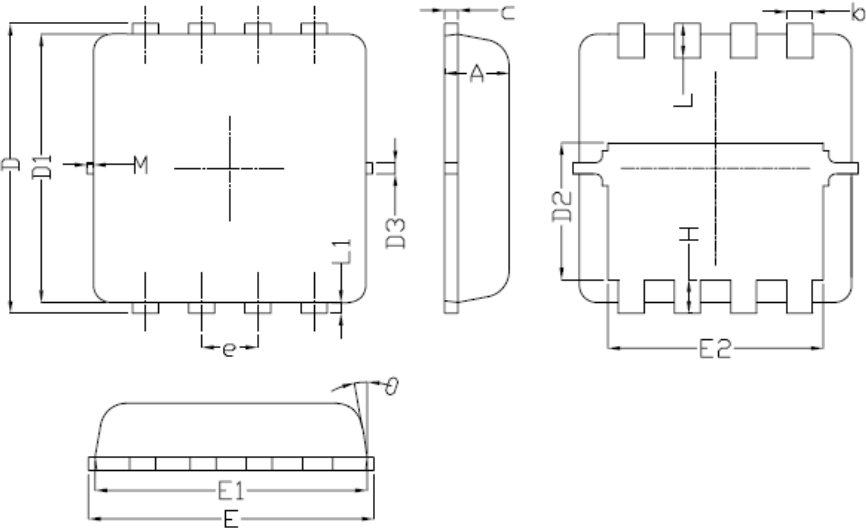
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{Amax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _p)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

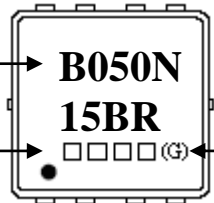
Note :1. All temperatures refer to topside of the package, measured on the package body surface.
 2. For devices mounted on FR-4 PCB of 1.6mm or equivalent grade PCB. If other grade PCB is used, care should be taken to match the coefficients of thermal expansion between components and PCB. If they are not matched well, the solder joints may crack or the bodies of the parts may crack or shatter as the assembly cools.

DFN3x3 Dimension



Marking:

D D D D



Device Code: **B050N**
 Date Code: **15BR**
 Assembly site code: S S S G

blank → JCET
 G → GEM

8-Lead DFN3x3 Plastic Package
CYStek Package Code: V8

Date Code(counting from left to right) :
 1st code: year code, the last digit of Christian year
 2nd code : month code, Jan→A, Feb→B, Mar→C, Apr→D
 May→E, Jun→F, Jul→G, Aug→H, Sep→J,
 Oct→K, Nov→L, Dec→M
 3rd and 4th codes : production serial number, 01~99

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.70	0.80	0.028	0.031	E1	3.00	3.20	0.118	0.126
b	0.25	0.35	0.010	0.014	E2	2.39	2.59	0.094	0.102
c	0.10	0.25	0.004	0.010	e	0.65 BSC		0.026 BSC	
D	3.25	3.45	0.128	0.136	H	0.30	0.50	0.012	0.020
D1	3.00	3.20	0.118	0.126	L	0.30	0.50	0.012	0.020
D2	1.48	1.68	0.058	0.066	L1	0.13 TYP		0.005 TYP	
D3	0.13 TYP		0.005 TYP		θ	8°	12°	8°	12°
E	3.20	3.40	0.126	0.134	M	-	0.15	-	0.006

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.