

N-Channel Enhancement Mode Power MOSFET

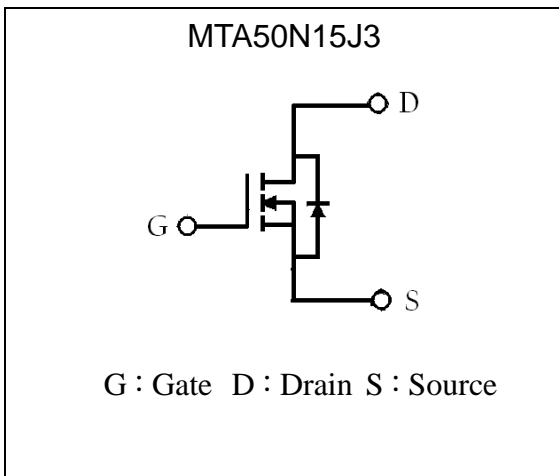
MTA50N15J3

BV_{DSS}	150V
I_D@T_C=25°C, V_{GS}=10V	27A
R_{DS(ON)}@ V_{GS}=10V, I_D=15A	44.3 mΩ (typ)
R_{DS(ON)}@ V_{GS}=4.5V, I_D=10A	43.0 mΩ (typ)

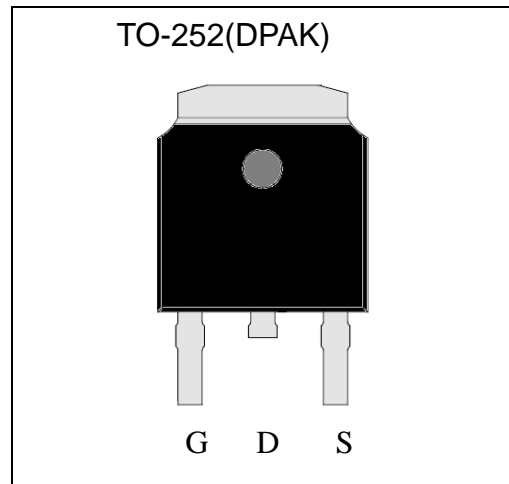
Features

- Low On Resistance
- Simple Drive Requirement
- Low Gate Charge
- Fast Switching Characteristic
- RoHS compliant package

Symbol

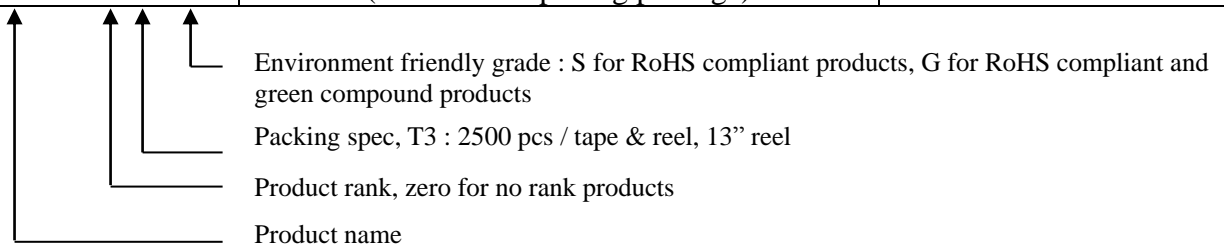


Outline



Ordering Information

Device	Package	Shipping
MTA50N15J3-0-T3-X	TO-252 (Pb-free lead plating package)	2500 pcs / Tape & Reel



**Absolute Maximum Ratings** ($T_C=25^{\circ}\text{C}$)

Parameter	Symbol	Limits	Unit
Drain-Source Voltage (Note 1)	V_{DS}	150	V
Gate-Source Voltage	V_{GS}	± 16	
Continuous Drain Current @ $T_C=25^{\circ}\text{C}$, $V_{GS}=10\text{V}$ (Note 1)	I_D	27	A
Continuous Drain Current @ $T_C=100^{\circ}\text{C}$, $V_{GS}=10\text{V}$ (Note 1)		19	
Continuous Drain Current @ $T_A=25^{\circ}\text{C}$, $V_{GS}=10\text{V}$ (Note 4)	I_{DSM}	4.0	
Continuous Drain Current @ $T_A=70^{\circ}\text{C}$, $V_{GS}=10\text{V}$ (Note 4)		3.2	
Pulsed Drain Current @ $V_{GS}=10\text{V}$ (Note 3)	I_{DM}	100	
Avalanche Current @ $L=0.1\text{mH}$ (Note 3)	I_{AS}	13	
Single Pulse Avalanche Energy @ $L=1\text{mH}$, $I_D=13\text{Amps}$, $V_{DD}=50\text{V}$ (Note 5)	E_{AS}	84	
Power Dissipation	P_D	$T_C=25^{\circ}\text{C}$ (Note 1)	100
		$T_C=100^{\circ}\text{C}$ (Note 1)	50
	P_{DSM}	$T_A=25^{\circ}\text{C}$ (Note 2)	2
		$T_A=70^{\circ}\text{C}$ (Note 2)	1.3
Operating Junction and Storage Temperature	T_j, T_{stg}	-55~+175	$^{\circ}\text{C/W}$

*Drain current limited by maximum junction temperature

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	$R_{th,j-c}$	1.5	$^{\circ}\text{C/W}$
Thermal Resistance, Junction-to-ambient, max (Note2)	$R_{th,j-a}$	62.5	
Thermal Resistance, Junction-to-ambient, max (Note4)		90	

Note : 1. The power dissipation P_D is based on $T_{J(MAX)}=175^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

2. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2 oz. copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C . The value in any given application depends on the user's specific board design.

3. Pulse width limited by junction temperature $T_{J(MAX)}=175^{\circ}\text{C}$. Ratings are based on low frequency and low duty cycles to keep initial $T_J=25^{\circ}\text{C}$.

4. When mounted on the minimum pad size recommended (PCB mount), $t \leq 10\text{s}$.

5. 100% tested by conditions of $L=0.1\text{mH}$, $I_{AS}=5\text{A}$, $V_{GS}=10\text{V}$, $V_{DD}=25\text{V}$



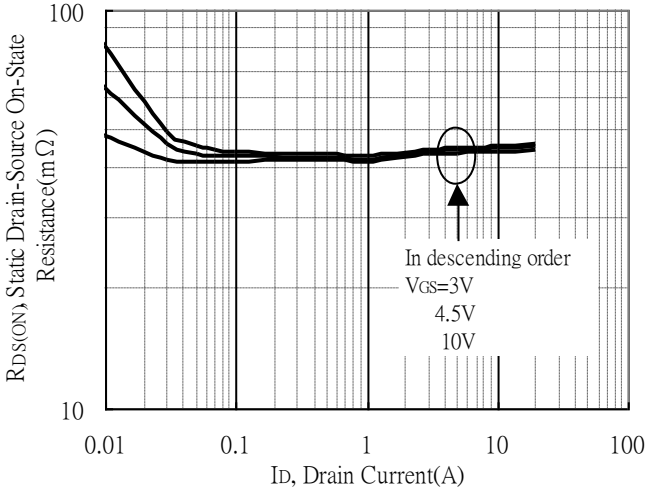
Characteristics (Tj=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	150	-	-	V	V _{GS} =0V, I _D =250μA
ΔBV _{DSS} /ΔT _j	-	0.1	-	V/°C	Reference to 25°C, I _D =250μA
V _{GS(th)}	0.5	-	1.2	V	V _{DS} = V _{GS} , I _D =250μA
*G _{FS}	-	43.5	-	S	V _{DS} =10V, I _D =10A
I _{GSS}	-	-	±100	nA	V _{GS} =±12V, V _{DS} =0V
I _{DSS}	-	-	1	μA	V _{DS} =120V, V _{GS} =0V
	-	-	25		V _{DS} =120V, V _{GS} =0V, T _j =125°C
*R _{DS(ON)}	-	44.3	56	mΩ	V _{GS} =10V, I _D =15A
	-	43.0	56		V _{GS} =4.5V, I _D =10A
Dynamic					
*Q _g	-	69.9	-	nC	I _D =15A, V _{DS} =120V, V _{GS} =10V
*Q _{gs}	-	3.8	-		
*Q _{gd}	-	12.5	-		
*t _{d(ON)}	-	11.6	-	ns	V _{DS} =75V, I _D =15A, V _{GS} =10V, R _G =6Ω
*t _r	-	21	-		
*t _{d(OFF)}	-	108.2	-		
*t _f	-	83.8	-		
C _{iss}	-	2161	-	pF	V _{GS} =0V, V _{DS} =80V, f=1MHz
C _{oss}	-	96	-		
C _{rss}	-	19	-		
R _g	-	1	-	Ω	f=1MHz
Source-Drain Diode					
*I _S	-	-	27	A	
*I _{SM}	-	-	100		
*V _{SD}	-	0.8	1.2	V	I _S =15A, V _{GS} =0V
*t _{rr}	-	41	-	ns	V _{GS} =0V, I _F =15A, dI _F /dt=100A/μs
*Q _{rr}	-	85	-	nC	

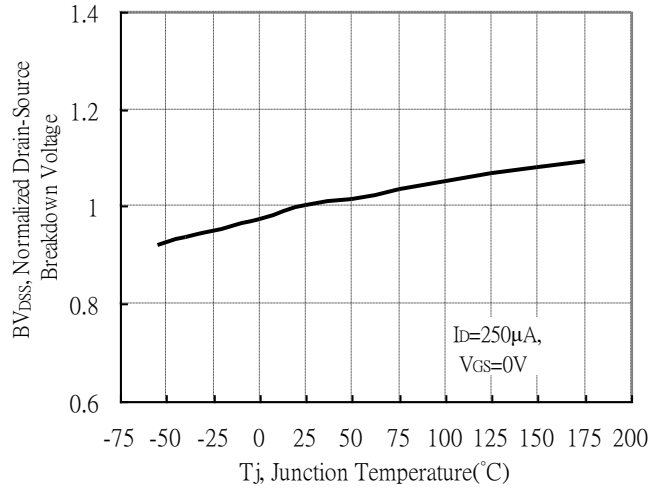
*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

Typical Characteristics

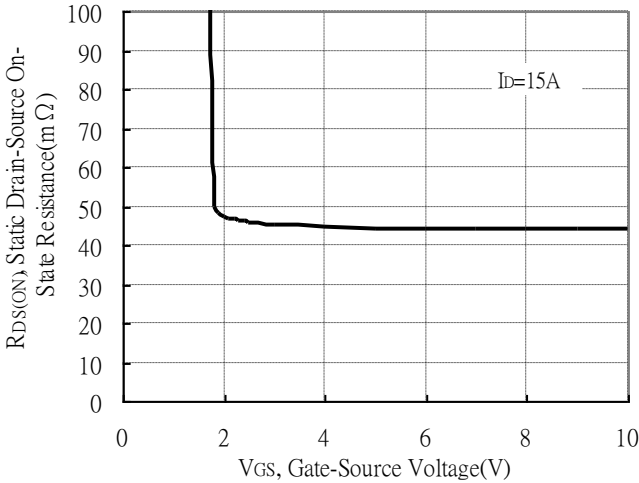
Static Drain-Source On-State resistance vs Drain Current



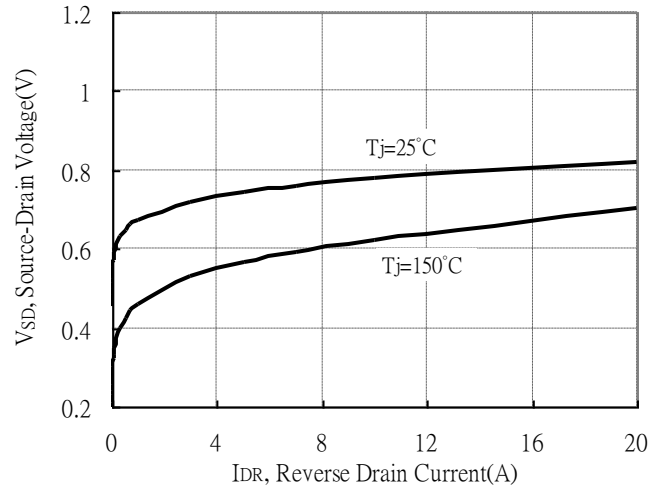
Brekdown Voltage vs Ambient Temperature



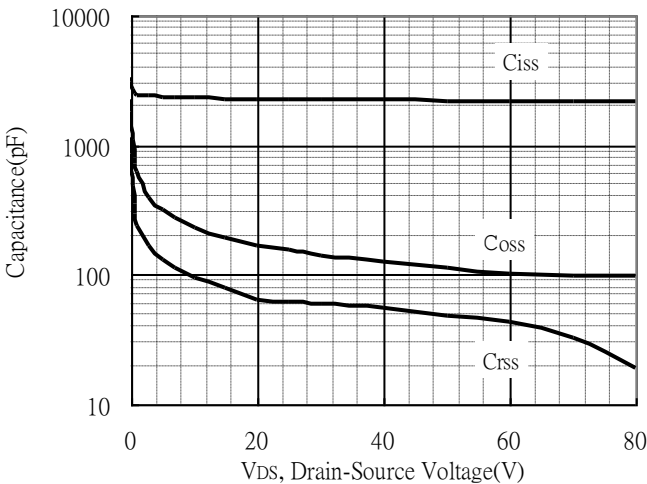
Static Drain-Source On-State Resistance vs Gate-Source Voltage



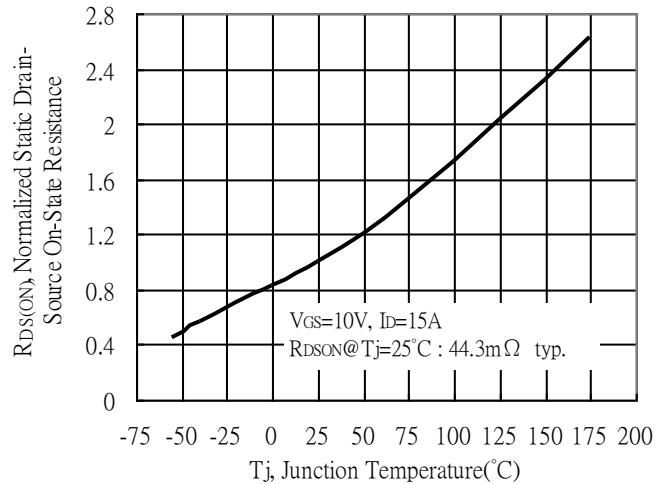
Reverse Drain Current vs Source-Drain Voltage



Capacitance vs Drain-to-Source Voltage

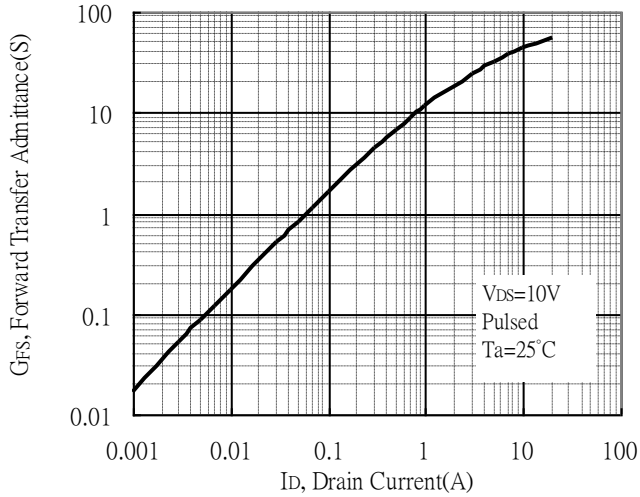


Drain-Source On-State Resistance vs Junction Temperature

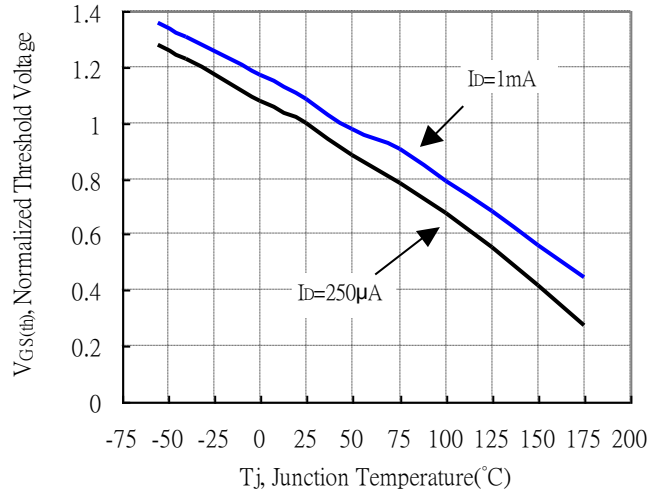


Typical Characteristics(Cont.)

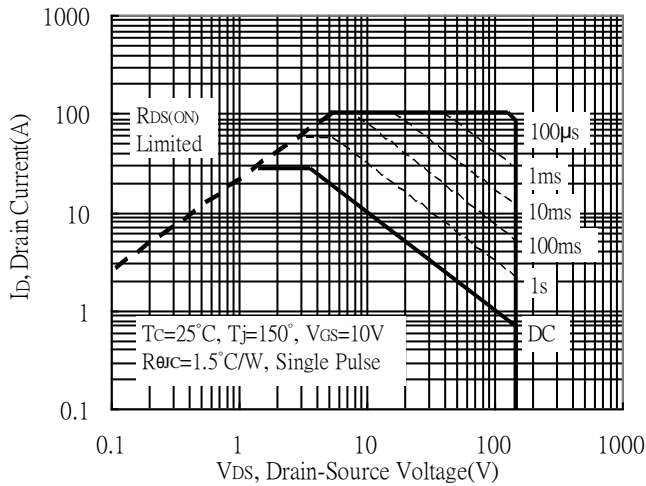
Forward Transfer Admittance vs Drain Current



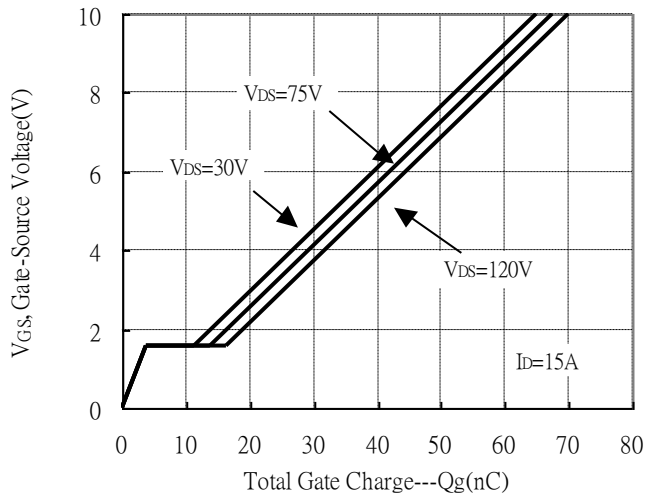
Normalized Threshold Voltage vs Junction Temperature



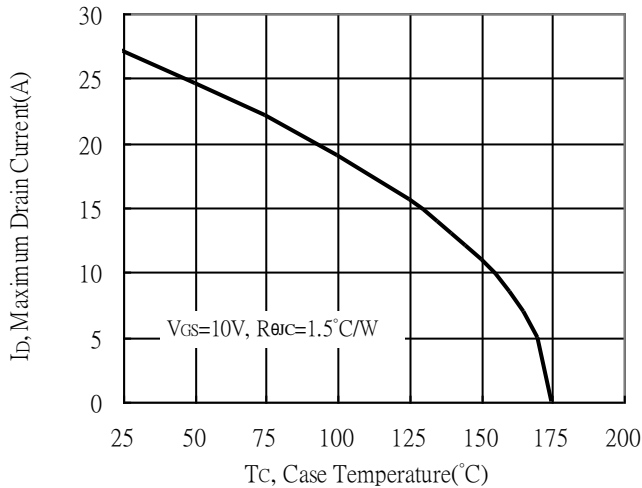
Maximum Safe Operating Area



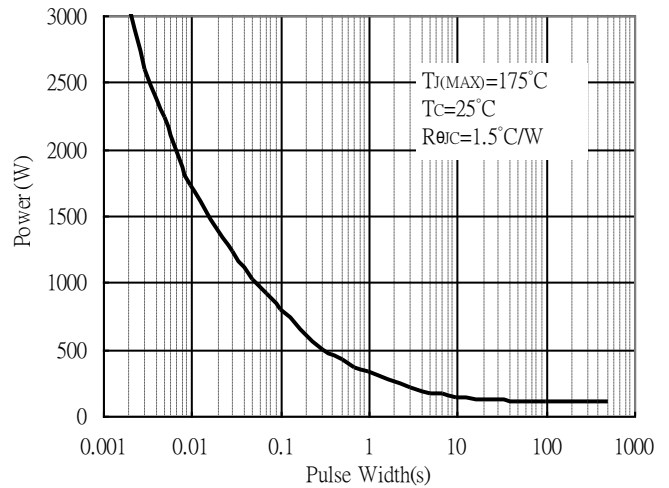
Gate Charge Characteristics



Maximum Drain Current vs Case Temperature

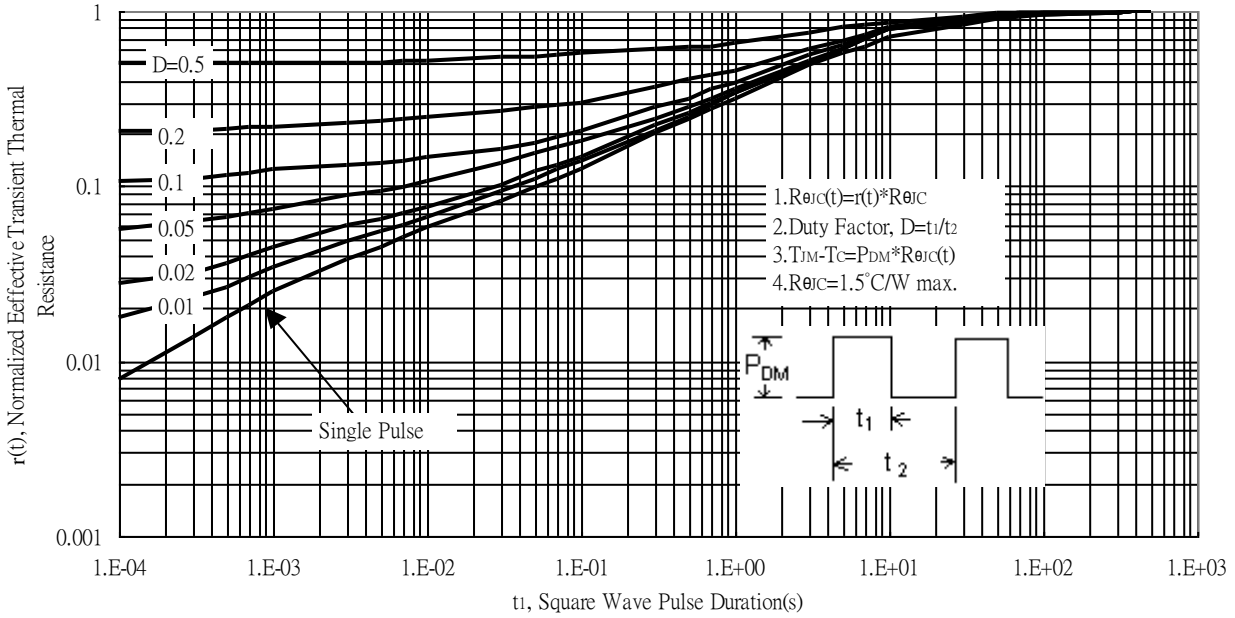


Single Pulse Maximum Power Dissipation

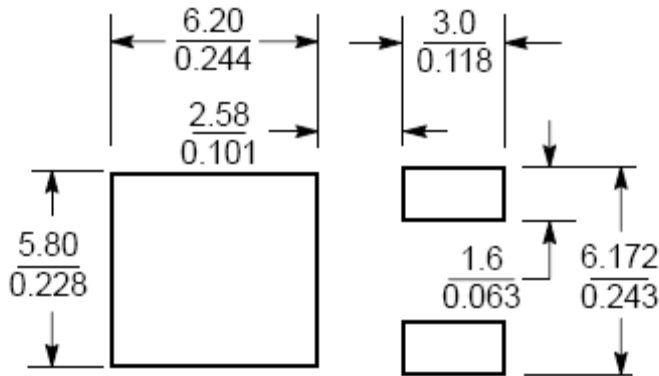


Typical Characteristics(Cont.)

Transient Thermal Response Curves

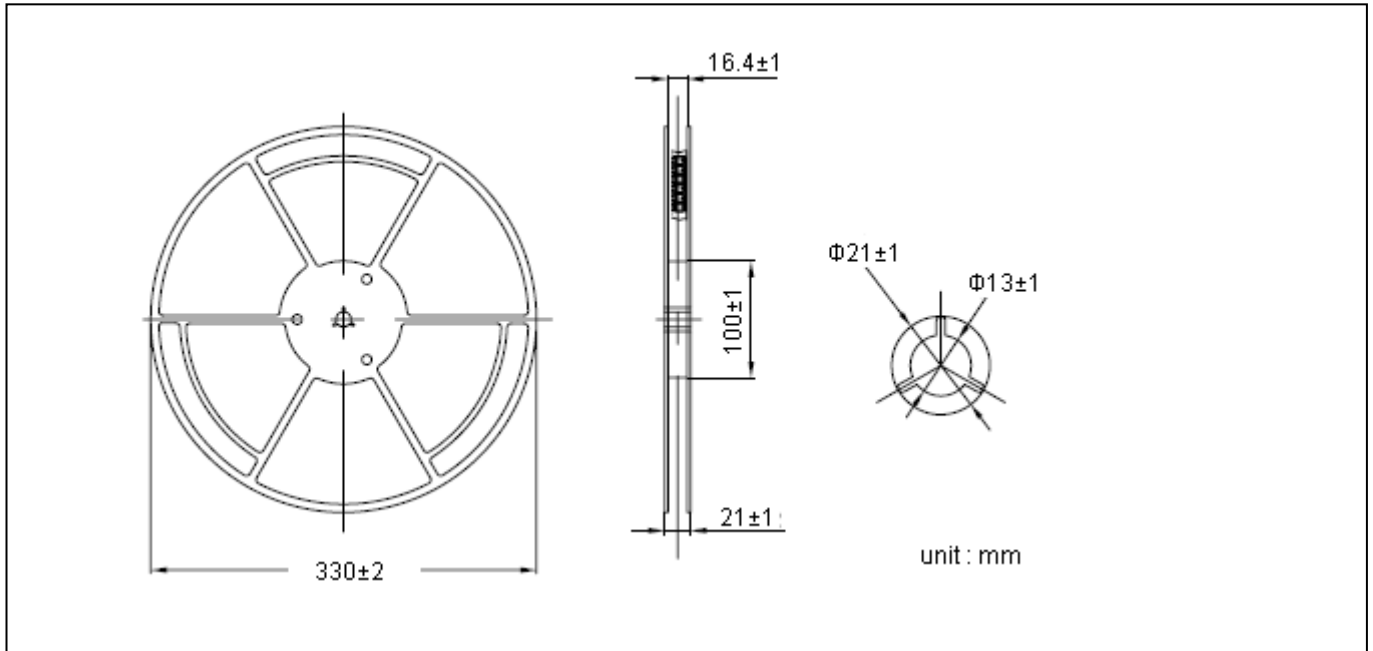


Recommended soldering footprint

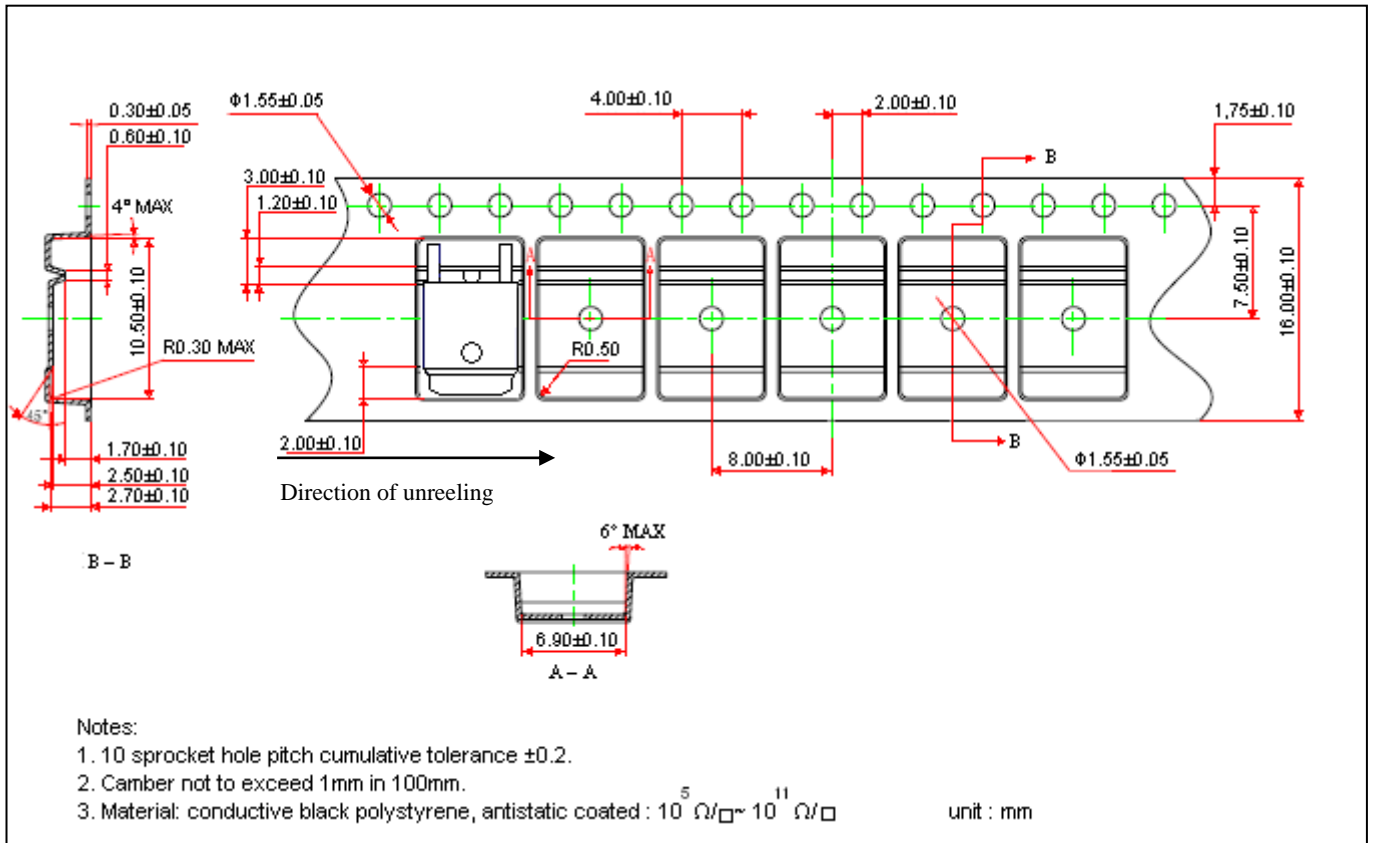


Unit ($\frac{\text{mm}}{\text{inch}}$)

Reel Dimension



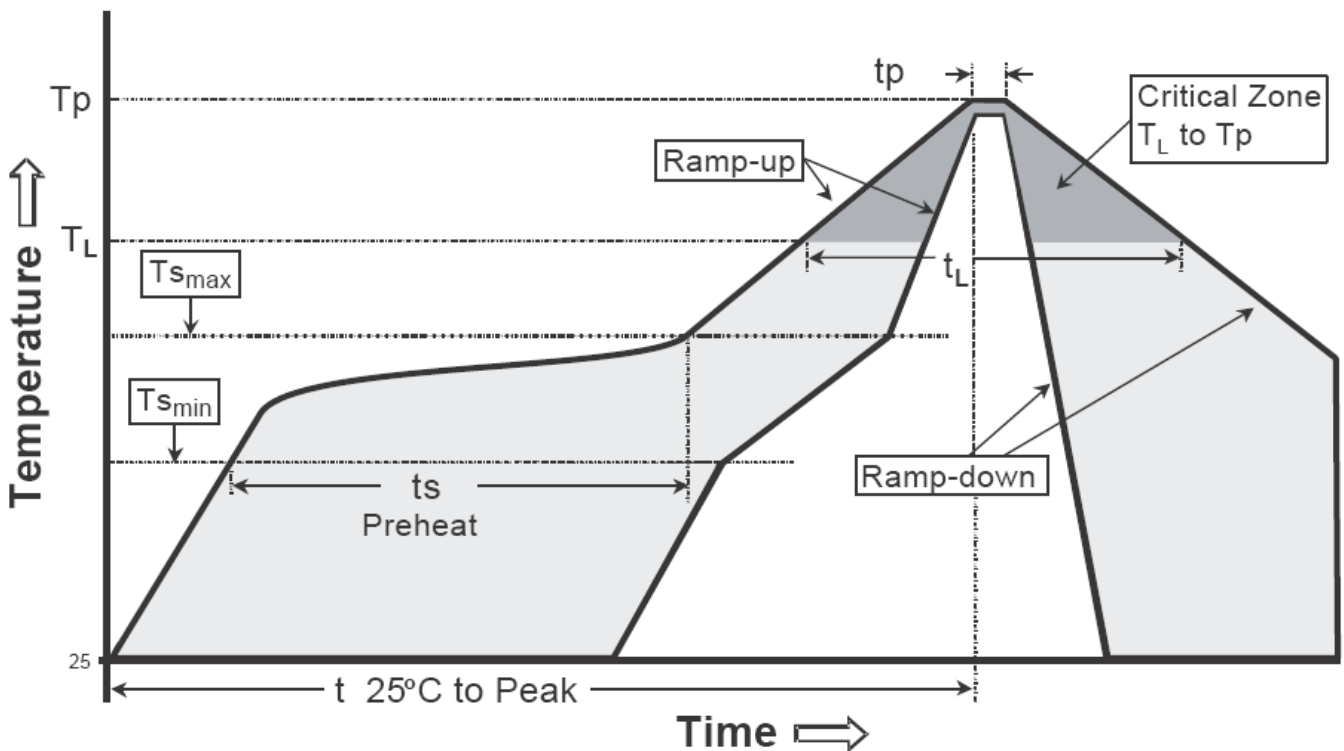
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

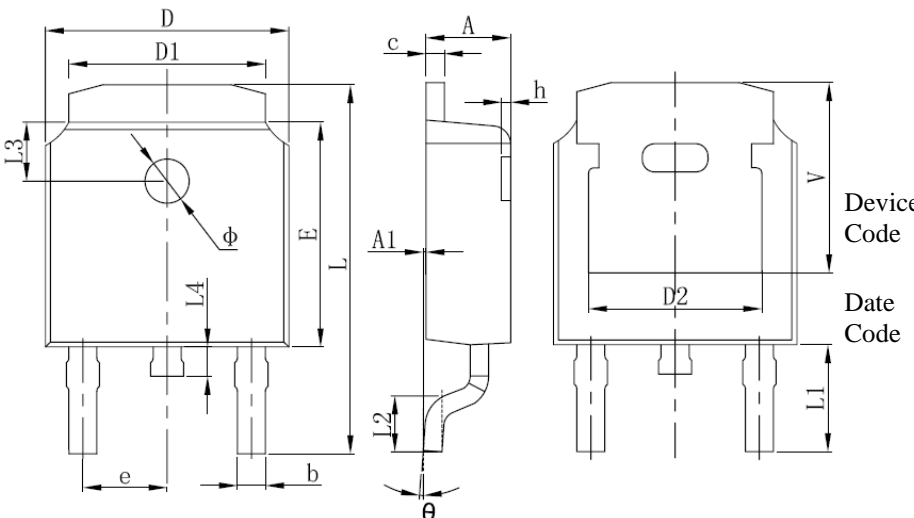
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _p)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-252 Dimension

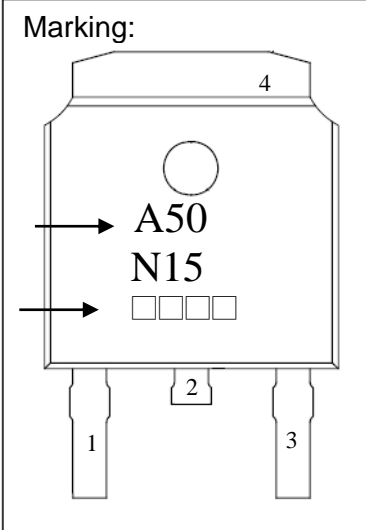


3-Lead TO-252 Plastic Surface Mount Package
 CYStek Package Code: J3

Date Code :
 First Code : Last digit of Christian Year
 Second Code : Month Code : Jan→A, Feb→B, Mar→C, Apr→D, May→E, Jun→F, Jul→G,
 Aug→H, Sep→J, Oct→K, Nov→L, Dec→M
 Last Two Codes : Production Serial Code, 01~99

Style: Pin 1.Gate 2.Drain 3.Source 4.Drain

Marking:



DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.087	0.094	2.200	2.400	L	0.382	0.406	9.712	10.312
A1	0.000	0.005	0.000	0.127	L1	0.114	REF	2.900	REF
b	0.025	0.030	0.635	0.770	L2	0.055	0.067	1.400	1.700
c	0.018	0.023	0.460	0.580	L3	0.063	REF	1.600	REF
D	0.256	0.264	6.500	6.700	L4	0.024	0.039	0.600	1.000
D1	0.201	0.215	5.100	5.460	Φ	0.043	0.051	1.100	1.300
D2	0.190	REF	4.830	REF	θ	0°	8°	0°	8°
E	0.236	0.244	6.000	6.200	h	0.000	0.012	0.000	0.300
e	0.086	0.094	2.186	2.386	v	0.207	REF	5.250	REF

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead : Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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