

**N-Channel Enhancement Mode Power MOSFET**

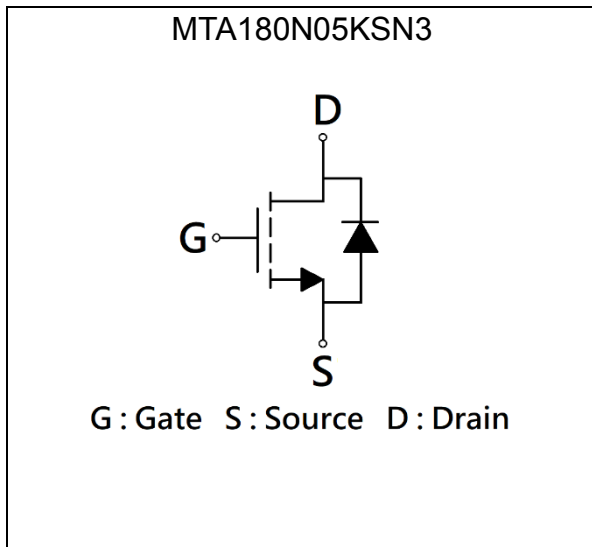
# MTA180N05KSN3

**Features**

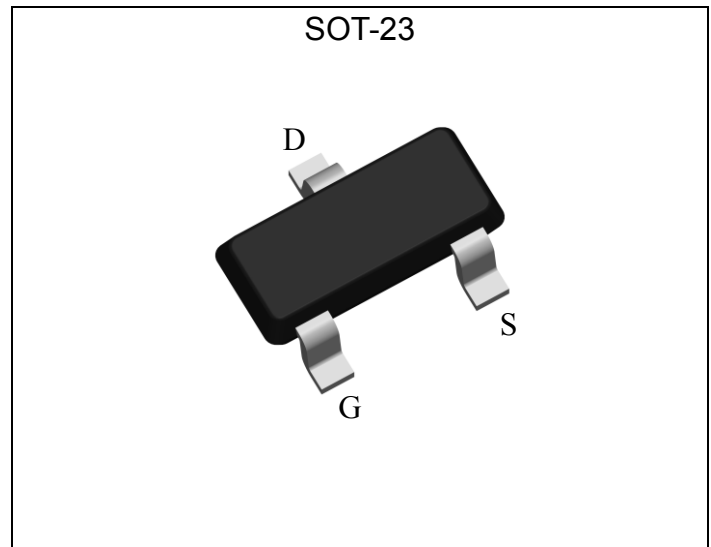
- Low On Resistance
- Low Gate Charge
- Fast Switching Characteristic
- ESD protected gate

$BV_{DSS}$	55V
$I_D @ V_{GS}=4.5V, T_A=25^\circ C$	1.5A
$R_{DS(ON) typ. @ V_{GS}=4.5V, I_D=1.5A}$	220m $\Omega$
$R_{DS(ON) typ. @ V_{GS}=2.5V, I_D=1.5A}$	320m $\Omega$

**Equivalent Circuit**

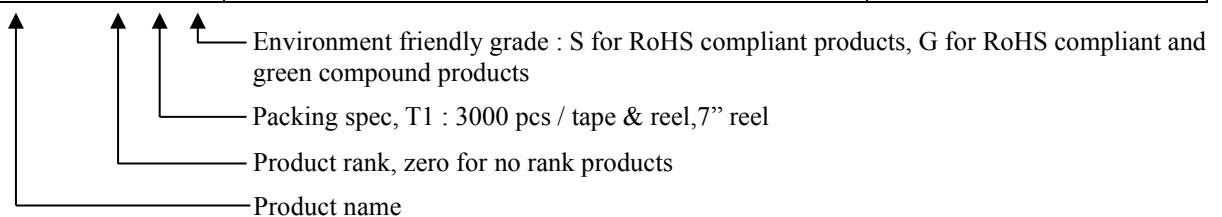


**Outline**



**Ordering Information**

Device	Package	Shipping
MTA180N05KSN3-0-T1-G	SOT-23 (Pb-free lead plating and halogen-free package)	3000 pcs / Tape & Reel



**Absolute Maximum Ratings (T<sub>A</sub>=25°C)**

Parameter	Symbol	Limits	Unit	
Drain-Source Voltage	V <sub>DS</sub>	55	V	
Gate-Source Voltage	V <sub>GS</sub>	±20		
Continuous Drain Current @ V <sub>GS</sub> =10V, T <sub>A</sub> =25°C	I <sub>D</sub>	1.5	A	
Continuous Drain Current @ V <sub>GS</sub> =10V, T <sub>A</sub> =70°C		1.2		
Pulsed Drain Current	I <sub>DM</sub>	6		
Continuous Body Diode Forward Current @ T <sub>A</sub> =25°C	I <sub>S</sub>	1		
Total Power Dissipation	P <sub>D</sub>	T <sub>A</sub> =25°C	1.3	W
		T <sub>A</sub> =70°C	0.8	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55~+150	°C	

**Thermal Data**

Parameter	Symbol	Steady State	Unit
Thermal Resistance, Junction-to-ambient	R <sub>θJA</sub>	100	°C/W

Note:

- \*a. The value of R<sub>θJA</sub> is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2 oz. copper, in a still air environment with T<sub>A</sub>=25°C. The power dissipation P<sub>D</sub> is based on R<sub>θJA</sub> and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.
- \*b. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150°C. Ratings are based on low frequency and low duty cycles to keep initial T<sub>J</sub>=25°C.



**Electrical Characteristics (T<sub>A</sub>=25°C, unless otherwise specified)**

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
<b>Static</b>					
BV <sub>DSS</sub>	55	-	-	V	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA
V <sub>GS(th)</sub>	0.5	-	1.5		V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA
G <sub>FS</sub>	-	4.5	-	S	V <sub>DS</sub> =5V, I <sub>D</sub> =5A
I <sub>GSS</sub>	-	-	±10	μA	V <sub>GS</sub> =±16V, V <sub>DS</sub> =0V
I <sub>DSS</sub>	-	-	1		V <sub>DS</sub> =44V, V <sub>GS</sub> =0V
R <sub>DS(ON)</sub>	-	220	290	mΩ	V <sub>GS</sub> =4.5V, I <sub>D</sub> =1.5A
	-	320	450		V <sub>GS</sub> =2.5V, I <sub>D</sub> =1.5A
<b>Dynamic</b>					
C <sub>iss</sub>	-	120	-	pF	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1MHz
C <sub>oss</sub>	-	16	-		
C <sub>rss</sub>	-	19	-		
R <sub>g</sub>	-	3.8	-	Ω	f=1MHz
Q <sub>g</sub> *1, 2	-	2	-	nC	V <sub>DS</sub> =25V, I <sub>D</sub> =1.5A, V <sub>GS</sub> =4.5V
Q <sub>gs</sub> *1, 2	-	0.7	-		
Q <sub>gd</sub> *1, 2	-	0.4	-		
t <sub>d(ON)</sub> *1, 2	-	5.5	-	ns	V <sub>DS</sub> =25V, I <sub>D</sub> =1.5A, V <sub>GS</sub> =4.5V, R <sub>GS</sub> =4.7Ω
t <sub>r</sub> *1, 2	-	17	-		
t <sub>d(OFF)</sub> *1, 2	-	11	-		
t <sub>f</sub> *1, 2	-	13	-		
<b>Source-Drain Diode</b>					
V <sub>SD</sub> *1	-	0.83	1.2	V	I <sub>S</sub> =1.5A, V <sub>GS</sub> =0V
t <sub>rr</sub>	-	7	-	ns	I <sub>F</sub> =1.5A, dI <sub>F</sub> /dt=100A/μs
Q <sub>rr</sub>	-	3	-	nC	

Note:

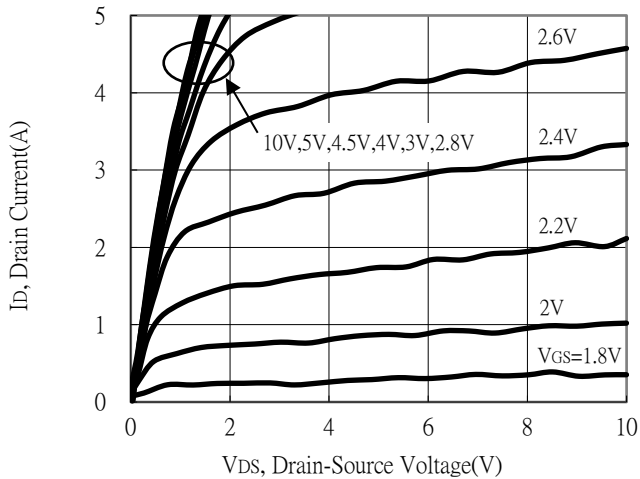
\*1. Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

\*2. Independent of operating temperature

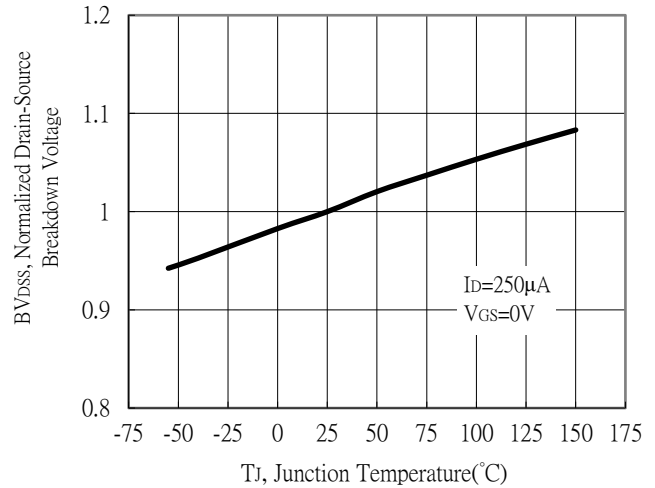


## Typical Characteristics

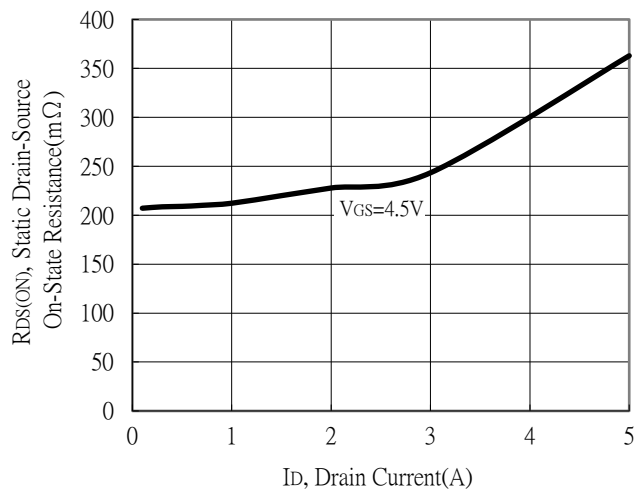
Typical Output Characteristics



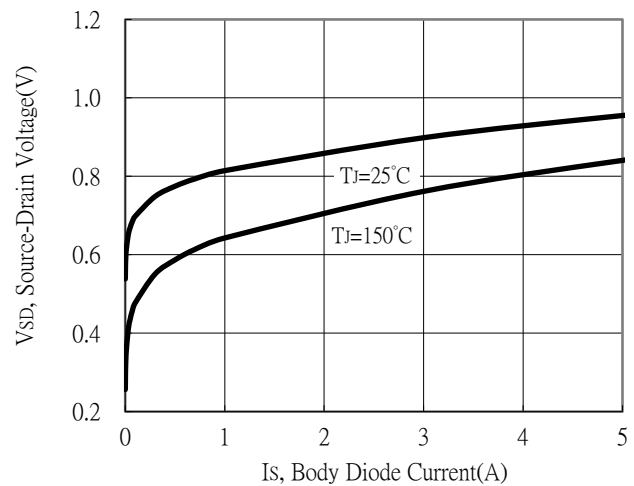
Breakdown Voltage vs Ambient Temperature



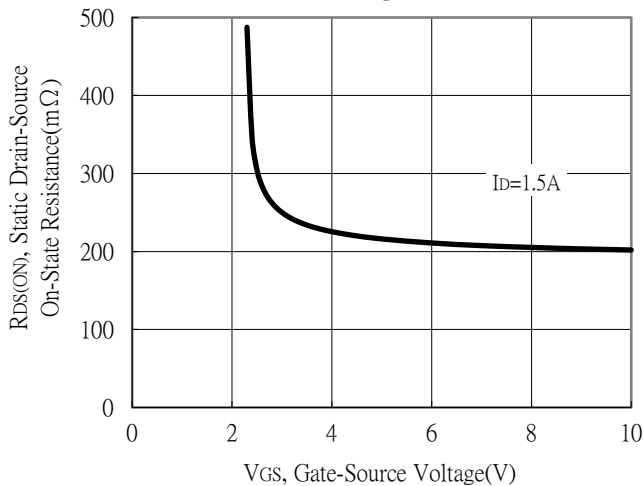
Static Drain-Source On-State resistance vs Drain Current



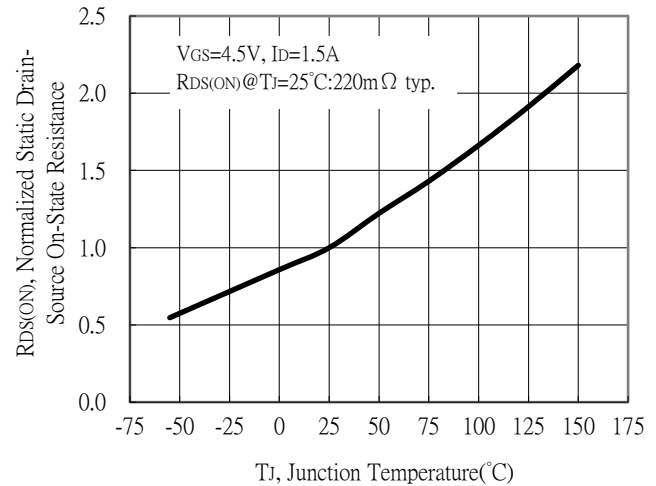
Body Diode Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

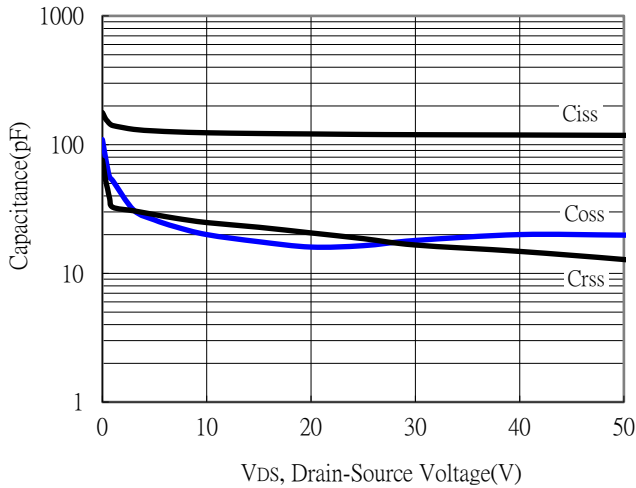


Drain-Source On-State Resistance vs Junction Temperature

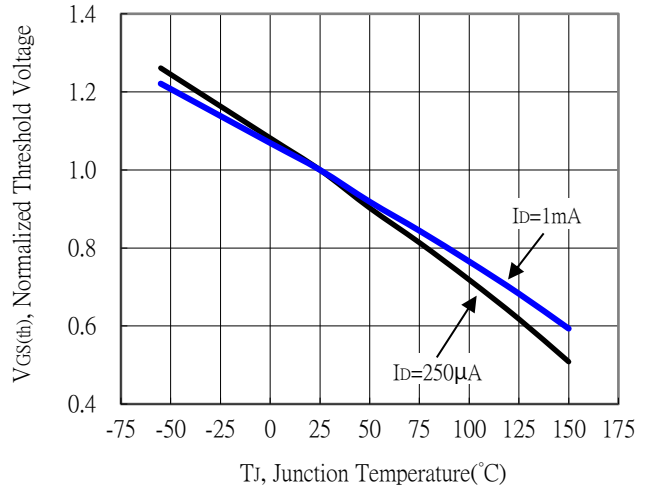


## Typical Characteristics (Cont.)

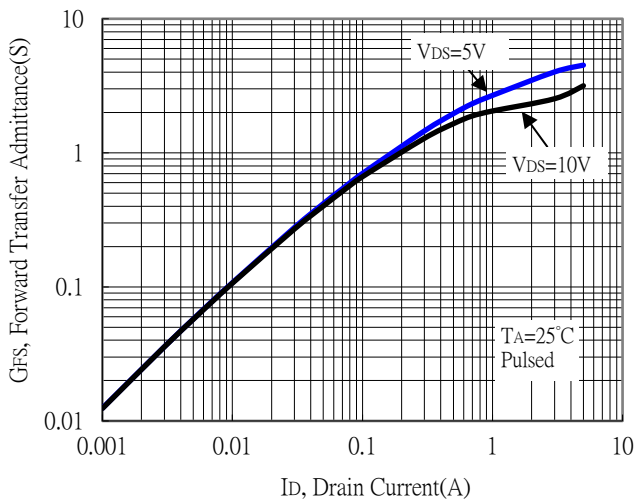
Capacitance vs Drain-to-Source Voltage



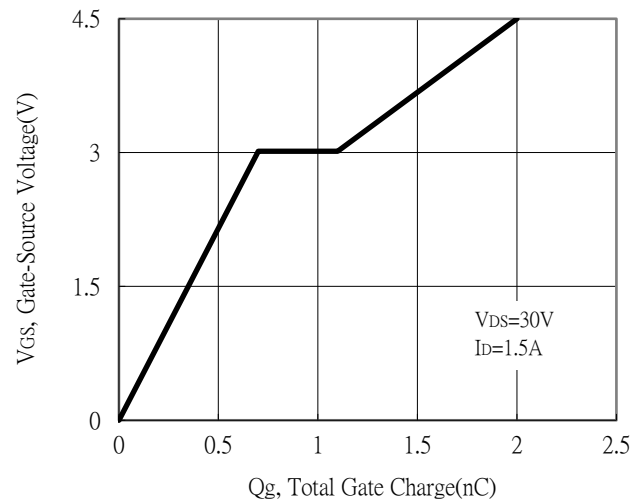
Threshold Voltage vs Junction Temperature



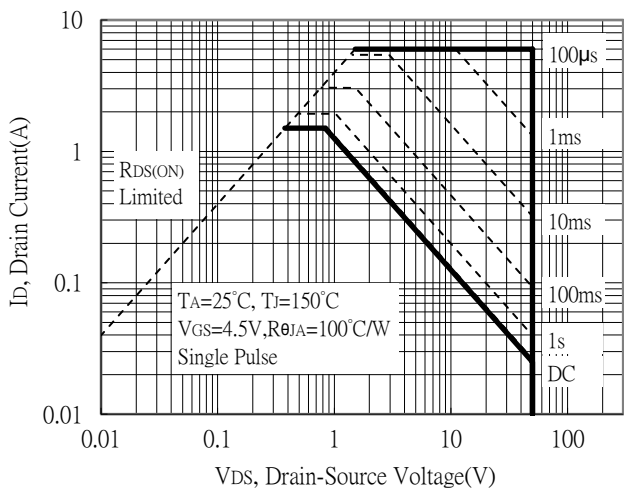
Forward Transfer Admittance vs Drain Current



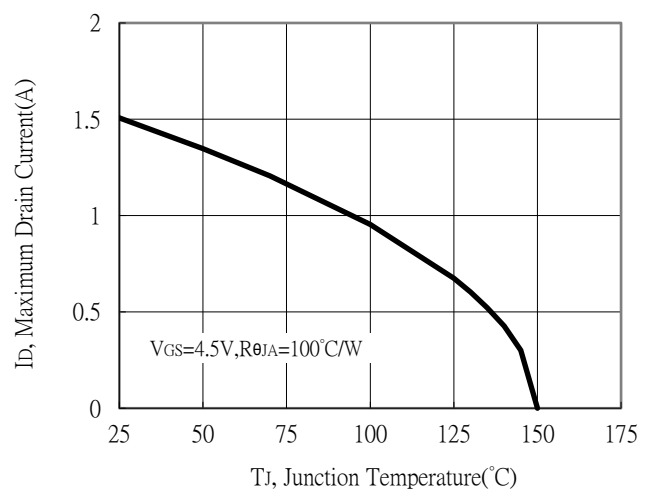
Gate Charge Characteristics



Maximum Safe Operating Area

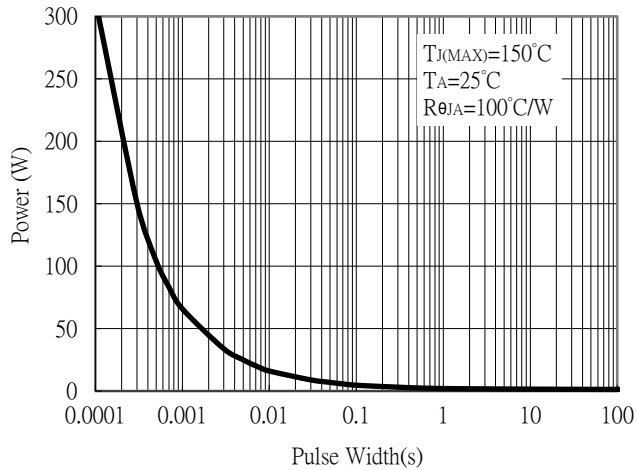


Maximum Drain Current vs Junction Temperature

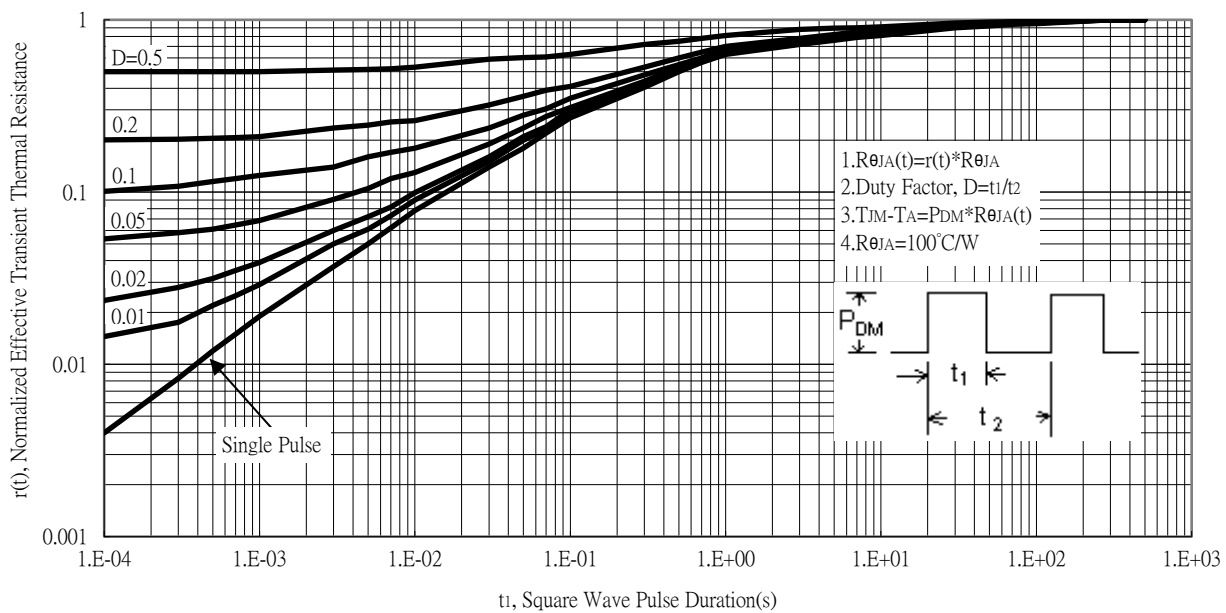


## Typical Characteristics (Cont.)

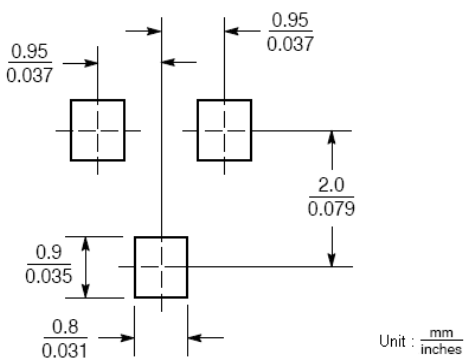
Single Pulse Power Rating, Junction to Ambient



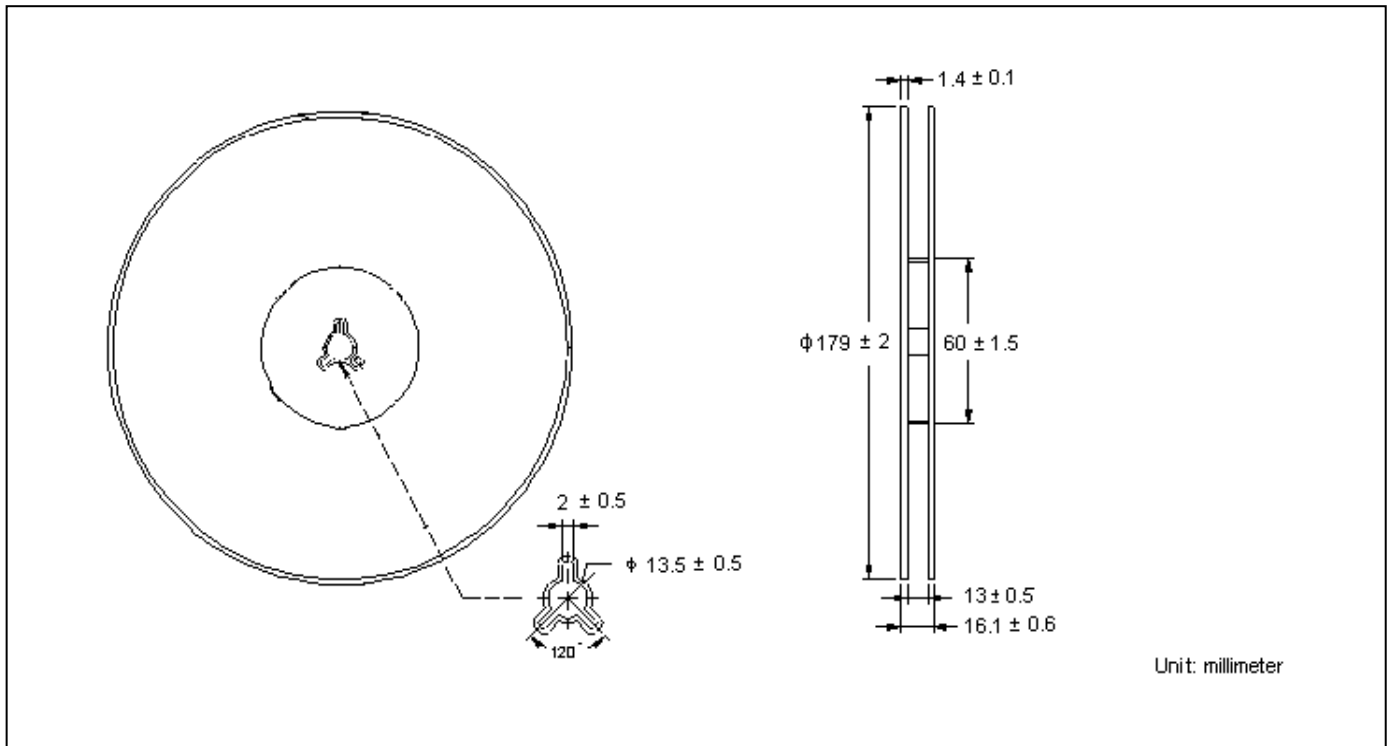
Transient Thermal Response Curves



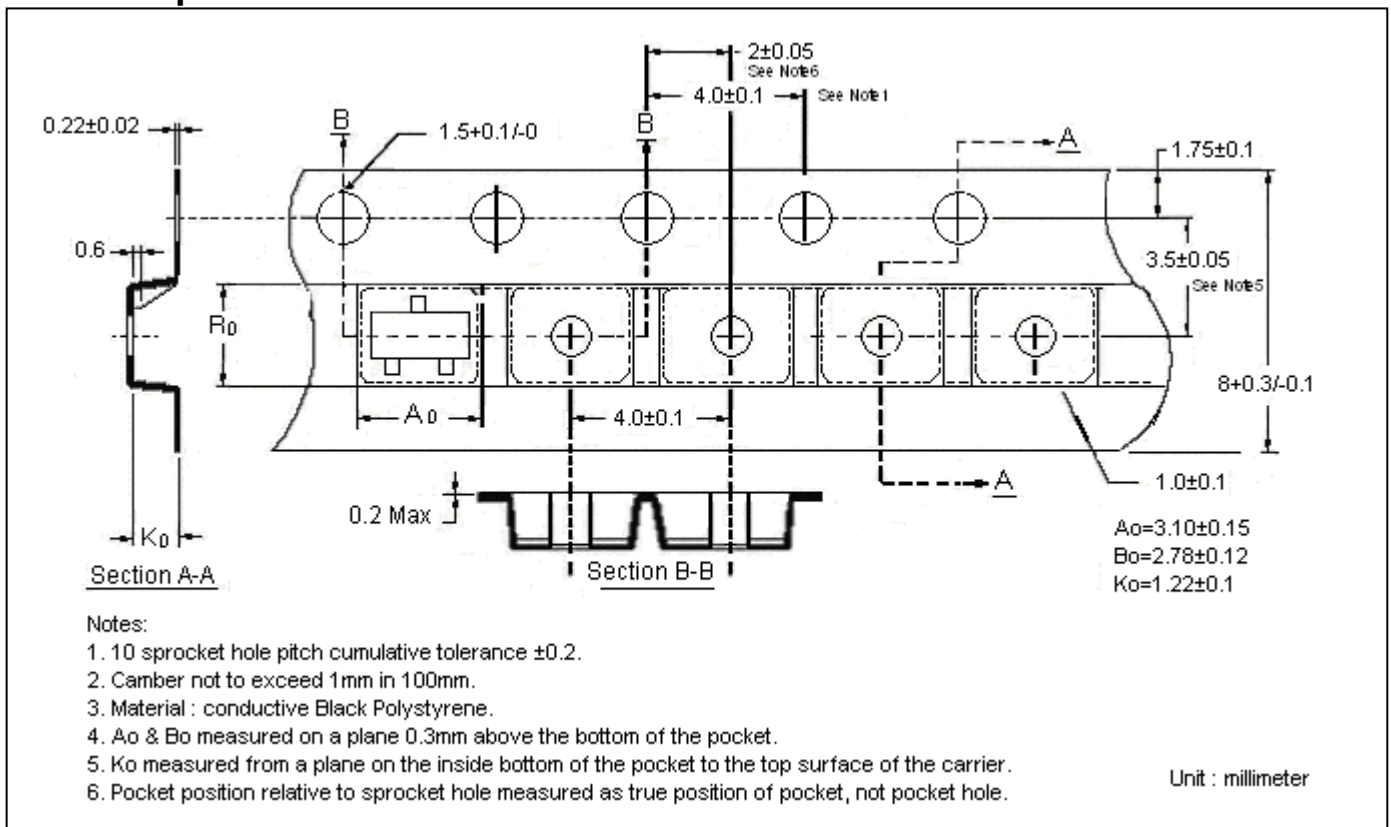
## Recommended Soldering Footprint



### Reel Dimension



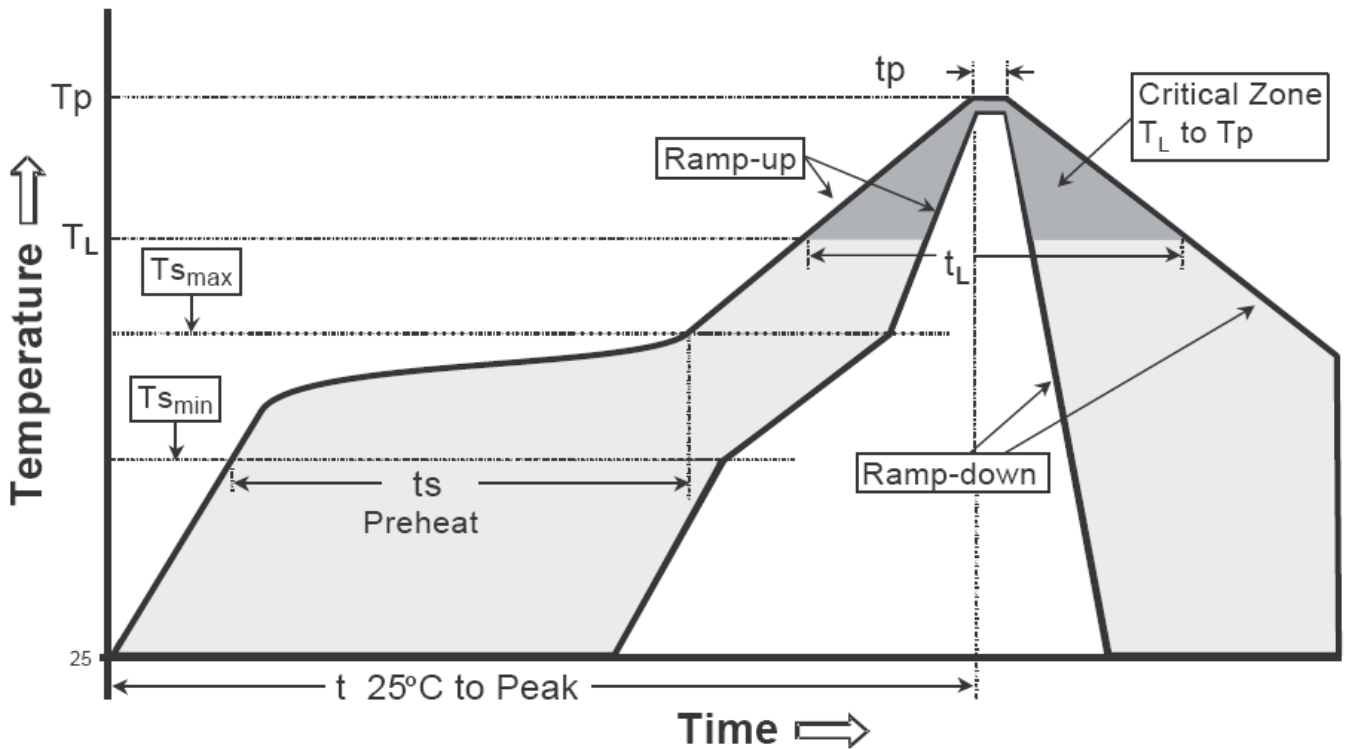
### Carrier Tape Dimension



**Recommended wave soldering condition**

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

**Recommended temperature profile for IR reflow**

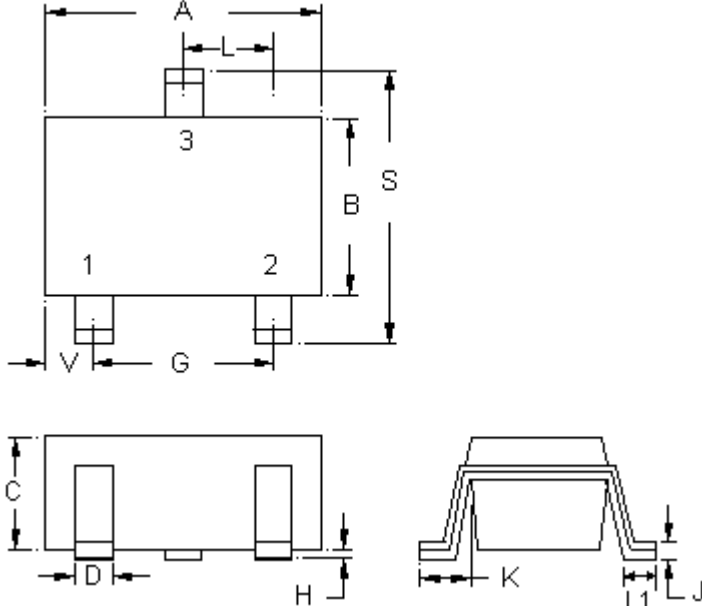


Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (Tl)	183°C	217°C
- Time (tl)	60-150 seconds	60-150 seconds
Peak Temperature(Tp)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

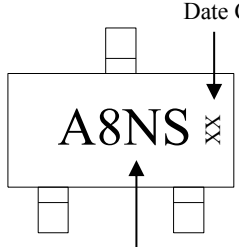


**SOT-23 Dimension**



The diagram shows three views of the SOT-23 package: a top view with dimensions A, L, B, S, 1, 2, 3, V, and G; a side view with dimensions C, D, and H; and a perspective view of the leads with dimensions K, L1, and L2.

**Marking:**



The marking diagram shows a rectangular package with three leads. The top surface is marked with 'A8NS' and 'XX'. Arrows indicate that 'A8NS' is the Device Code and 'XX' is the Date Code.

3-Lead SOT-23 Plastic Surface Mounted Package  
 CYStek Package Code: N3

Style: Pin      1.Gate      2.Source

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1102	0.1181	2.80	3.00	J	0.0032	0.0059	0.08	0.15
B	0.0472	0.0551	1.20	1.40	K	0.0217	REF	0.55	REF
C	0.0354	0.0413	0.90	1.05	L	0.0374	TYP	0.95	TYP
D	0.0118	0.0197	0.30	0.50	S	0.0886	0.1004	2.25	2.55
G	0.0709	0.0787	1.80	2.00	V	0.0098	0.0256	0.25	0.65
H	0.0000	0.0040	0.00	0.10	L1	0.0118	0.0197	0.30	0.50

**Notes:** 1.Controlling dimension: millimeters.  
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.  
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

**Material:**

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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