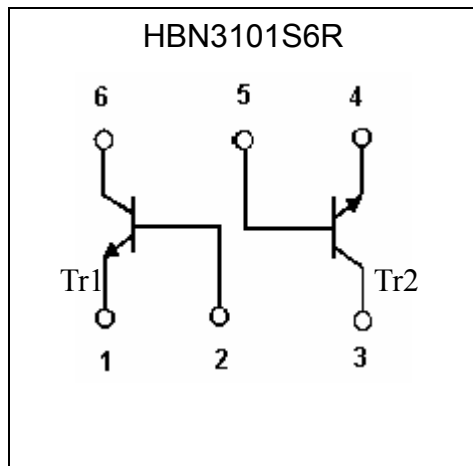


NPN Epitaxial Planar Transistor
HBN3101S6R
(Dual Transistors)

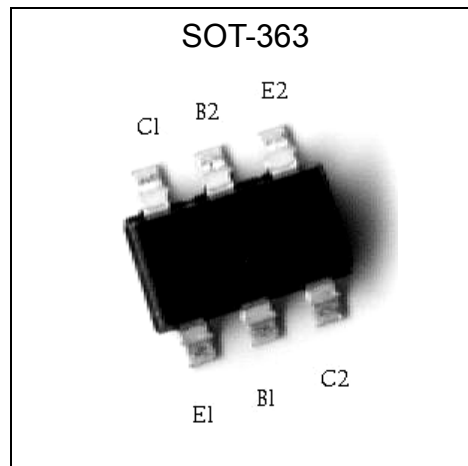
Features

- Two BF422 chips in a SOT-363 package.
- Mounting possible with SOT-323 automatic mounting machines.
- Transistor elements are independent, eliminating interference.
- Mounting cost and area can be cut in half.
- High BV_{CEO} , $BV_{CEO} \geq 300V$
- Pb-free lead plating and halogen-free package.

Equivalent Circuit

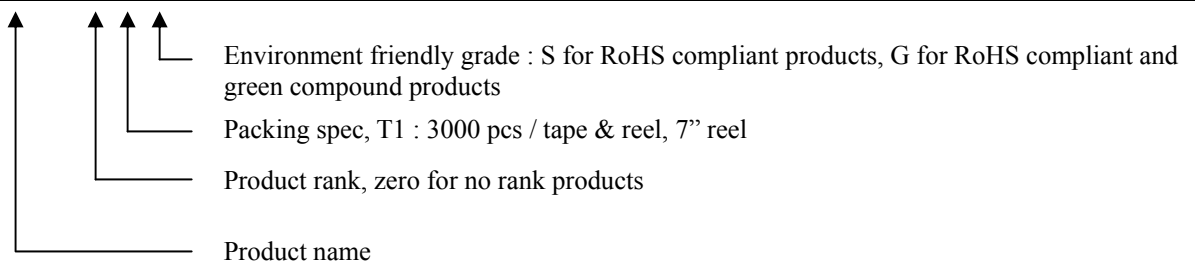


Outline



Ordering Information

Device	Package	Shipping
HBN3101S6R-0-T1-G	SOT-363 (Pb-free lead plating and halogen-free package)	3000 pcs / tape & reel



**The following characteristics apply to both Tr1 and Tr2****Absolute Maximum Ratings** (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V _{CBO}	300	V
Collector-Emitter Voltage	V _{CEO}	300	V
Emitter-Base Voltage	V _{EBO}	5	V
Collector Current (DC)	I _C	100	mA
Collector Current (Pulse)	I _{CP}	300 (Note 1)	mA
Power Dissipation	P _d	200 (total) (Note 2)	mW
Junction Temperature	T _j	150	°C
Storage Temperature	T _{stg}	-55~+150	°C

Note : 1.Single pulse, Pw=10ms
2.150mW per element must not be exceeded.

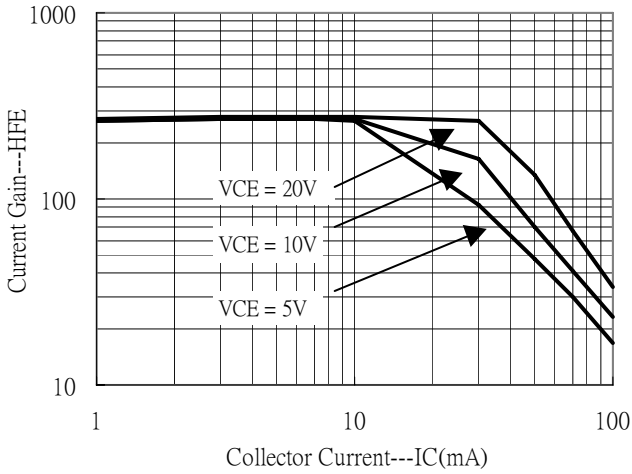
Characteristics (Ta=25°C)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV _{CBO}	300	-	-	V	I _C =100μA
BV _{CEO}	300	-	-	V	I _C =1mA
BV _{EBO}	5	-	-	V	I _E =10μA
I _{CBO}	-	-	100	nA	I _E =0, V _{CB} =300V
I _{EBO}	-	-	100	nA	V _{EB} =5V, I _C =0
*V _{CE(sat)}	-	-	300	mV	I _C =30mA, I _B =3mA
*V _{BE(sat)}	-	-	900	mV	I _C =30mA, I _B =3mA
*h _{FE1}	100	-	250	-	V _{CE} =5V, I _C =10mA
*h _{FE2}	15	-	-	-	V _{CE} =5V, I _C =50mA
f _T	60	-	-	MHz	V _{CE} =10V, I _C =10mA, f=100MHz
C _{ob}	-	-	15	pF	V _{CB} =10V, f=1MHz

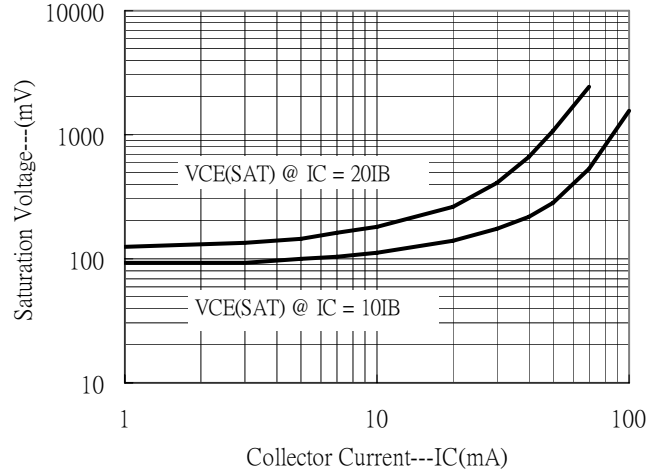
*Pulse Test : Pulse Width ≤380μs, Duty Cycle≤2%

Typical Characteristics

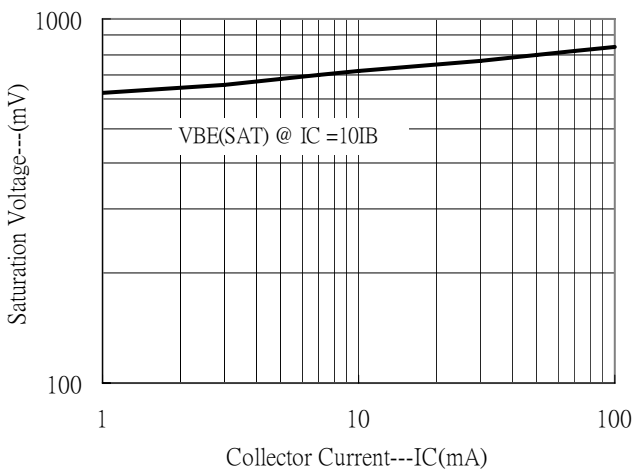
Current Gain vs Collector Current



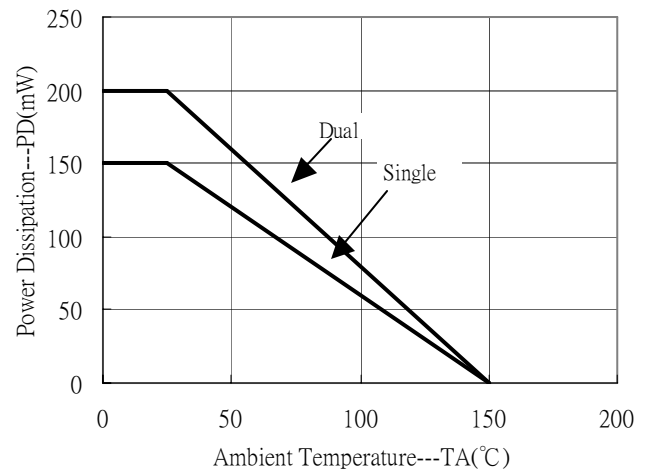
Saturation Voltage vs Collector Current



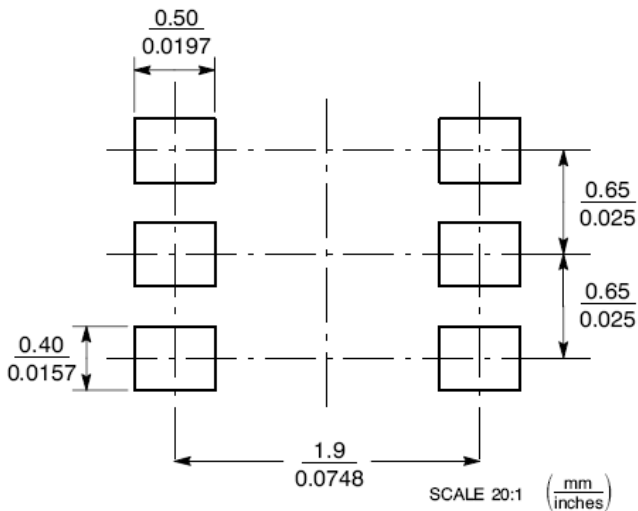
Saturation Voltage vs Collector Current



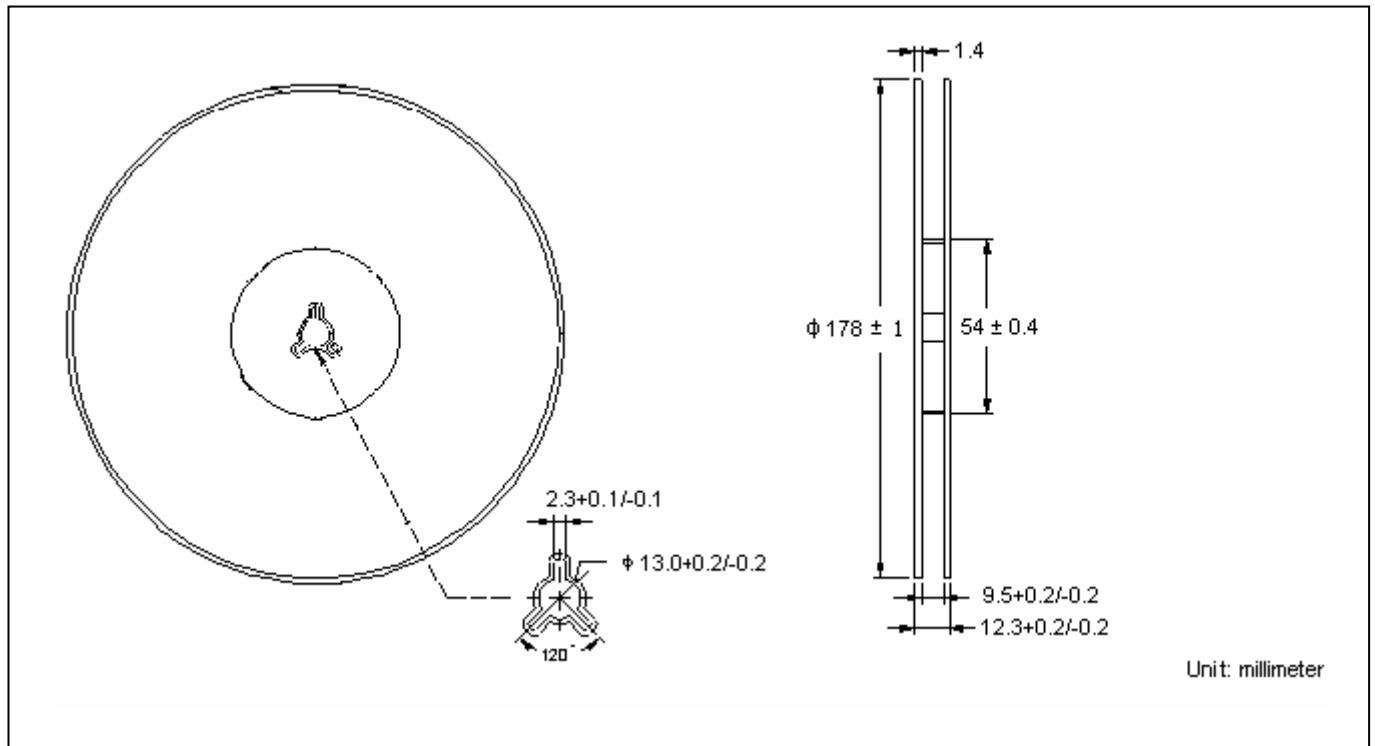
Power Derating Curves



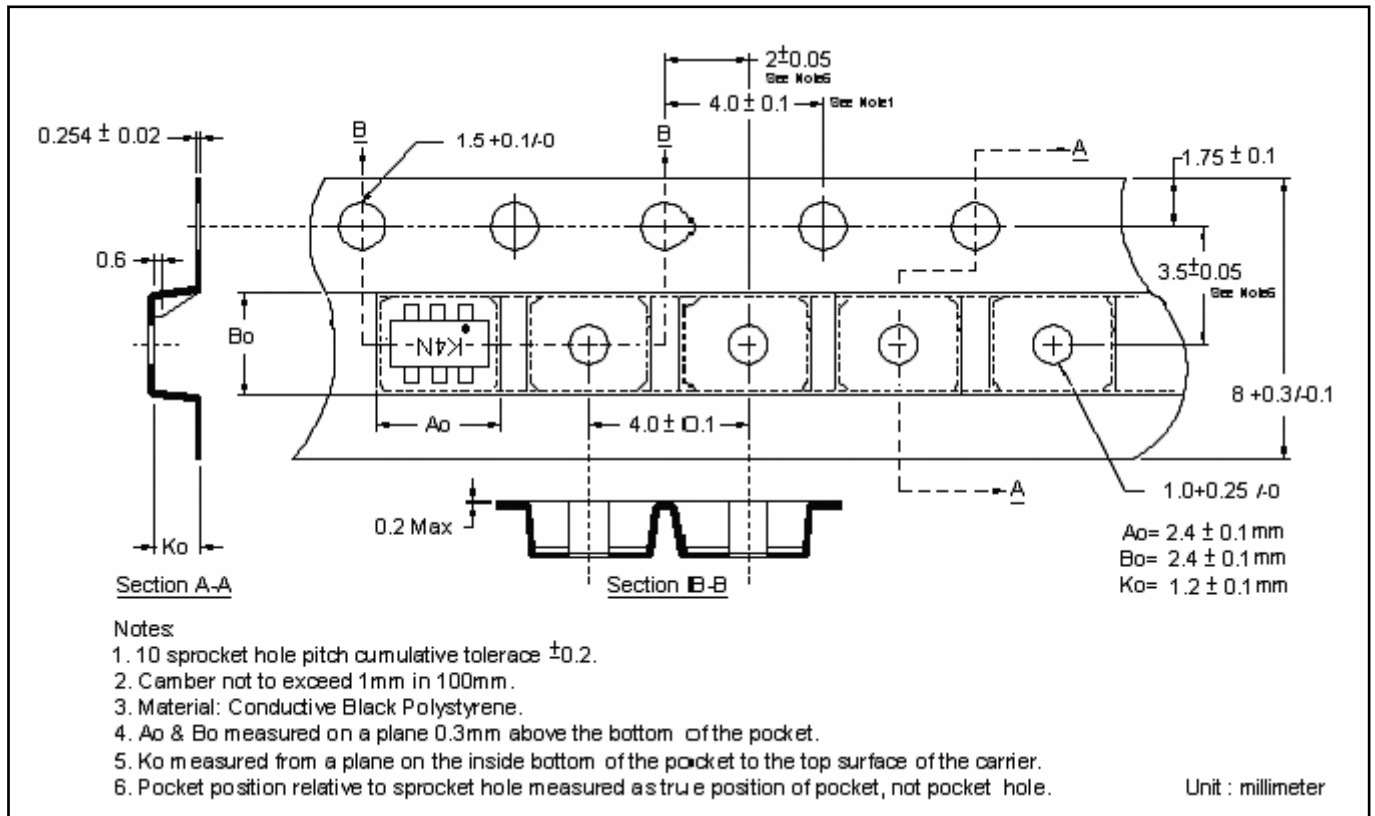
Recommended Soldering Footprint



Reel Dimension



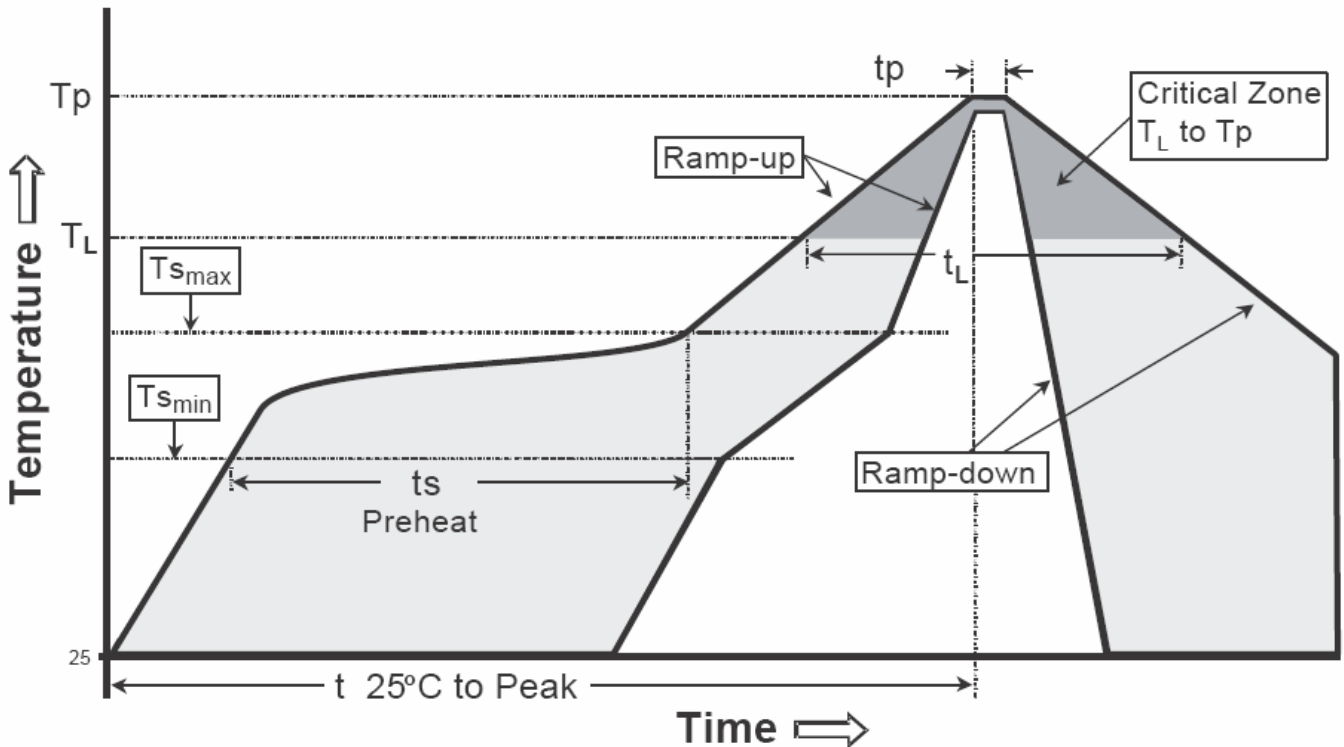
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

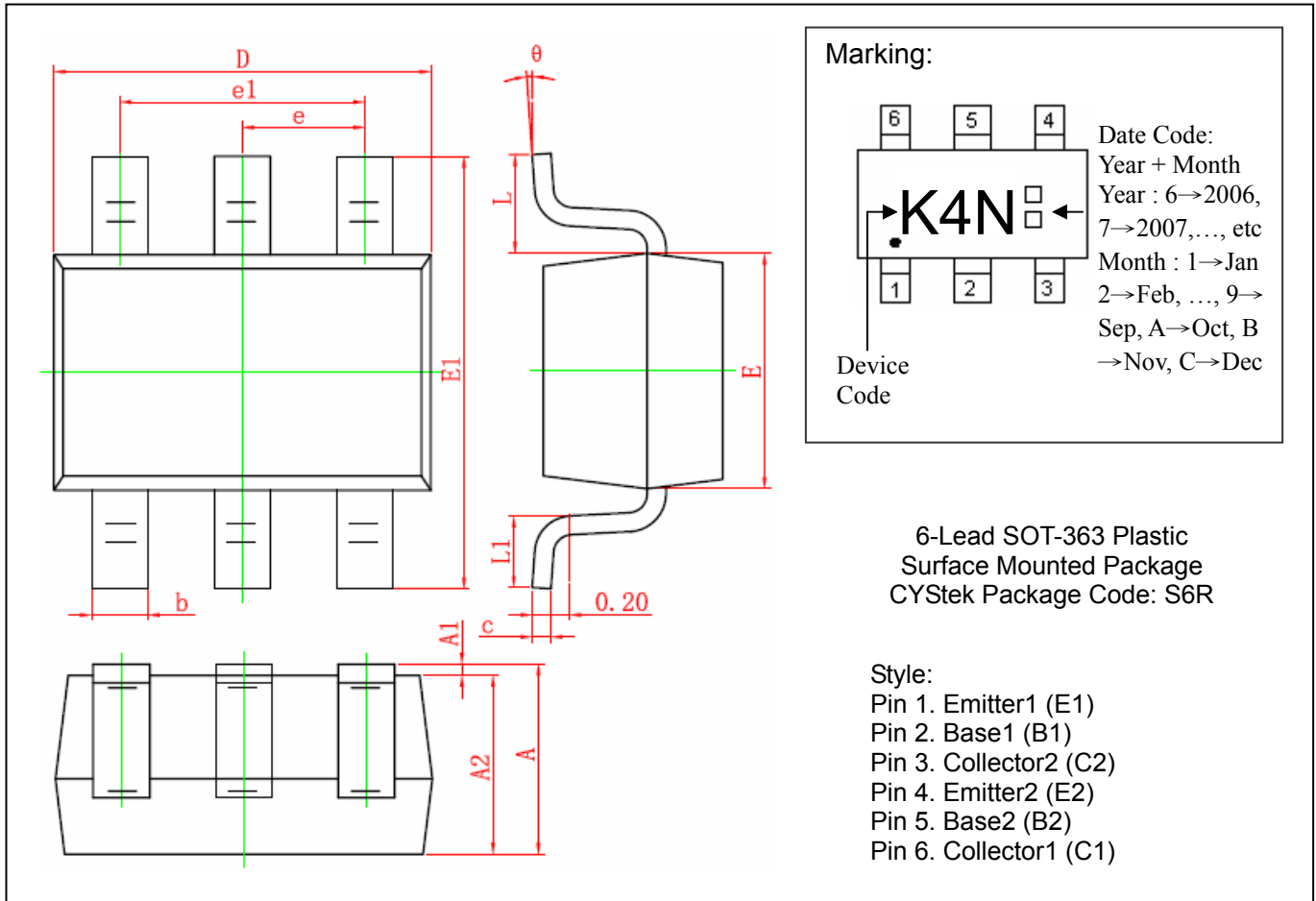
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

SOT-363 Dimension



DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.900	1.100	0.035	0.043	E1	2.150	2.450	0.085	0.096
A1	0.000	0.100	0.000	0.004	e	0.650	TYP	0.026	TYP
A2	0.900	1.000	0.035	0.039	e1	1.200	1.400	0.047	0.055
b	0.150	0.350	0.006	0.014	L	0.525	REF	0.021	REF
c	0.080	0.150	0.003	0.006	L1	0.260	0.460	0.010	0.018
D	2.000	2.200	0.079	0.087	θ	0°	8°	0°	8°
E	1.150	1.350	0.045	0.053					

Notes : 1. Controlling dimension : millimeters.
 2. Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3. If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material :

- Lead : Pure tin plated.
- Mold Compound : Epoxy resin family, flammability solid burning class:UL94V-0.

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