

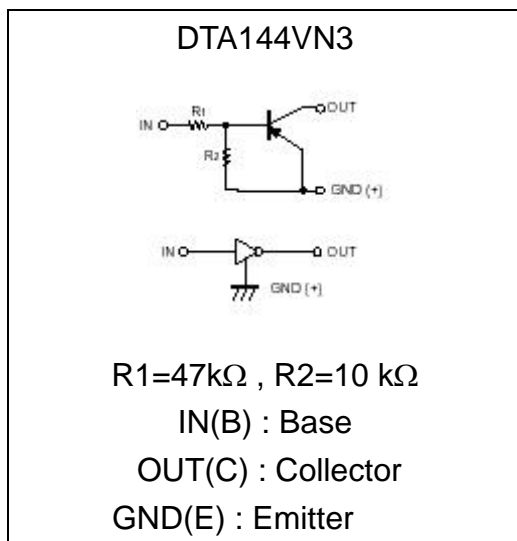
**General Purpose PNP Digital Transistors (Built-in Resistors)**

# DTA144VN3

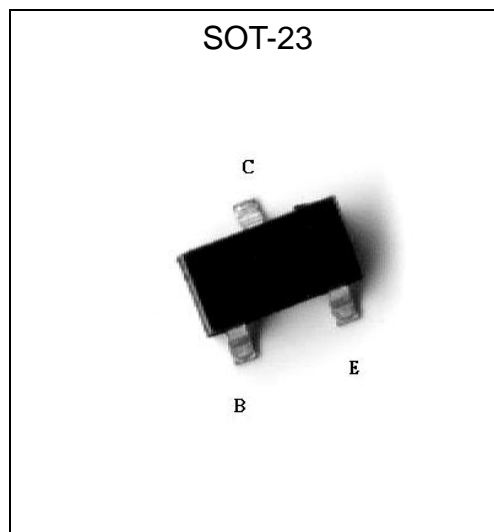
**Features**

- Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors (see equivalent circuit).
- The bias resistors consist of thin-film resistors with complete isolation to allow negative biasing of the input. They also have the advantage of almost completely eliminating parasitic effects.
- Only the on/off conditions need to be set for operation, making device design easy.
- Complements the DTC144VN3.
- Pb-free & Halogen-free package.

**Equivalent Circuit**

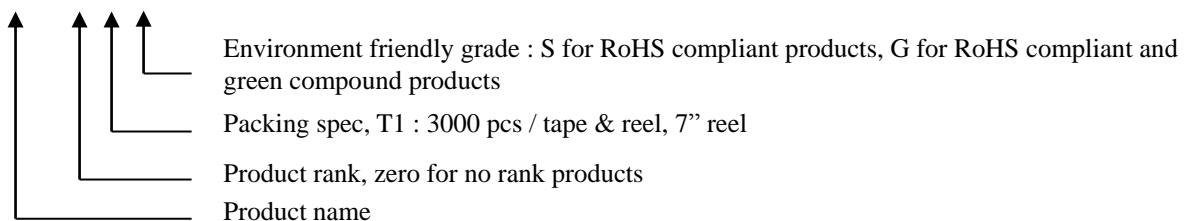


**Outline**



**Ordering Information**

Device	Package	Shipping
DTA144VN3-0-T1-G	SOT-23 (Pb-free lead plating and halogen-free package)	3000 pcs / tape & reel



**Absolute Maximum Ratings (Ta=25°C)**

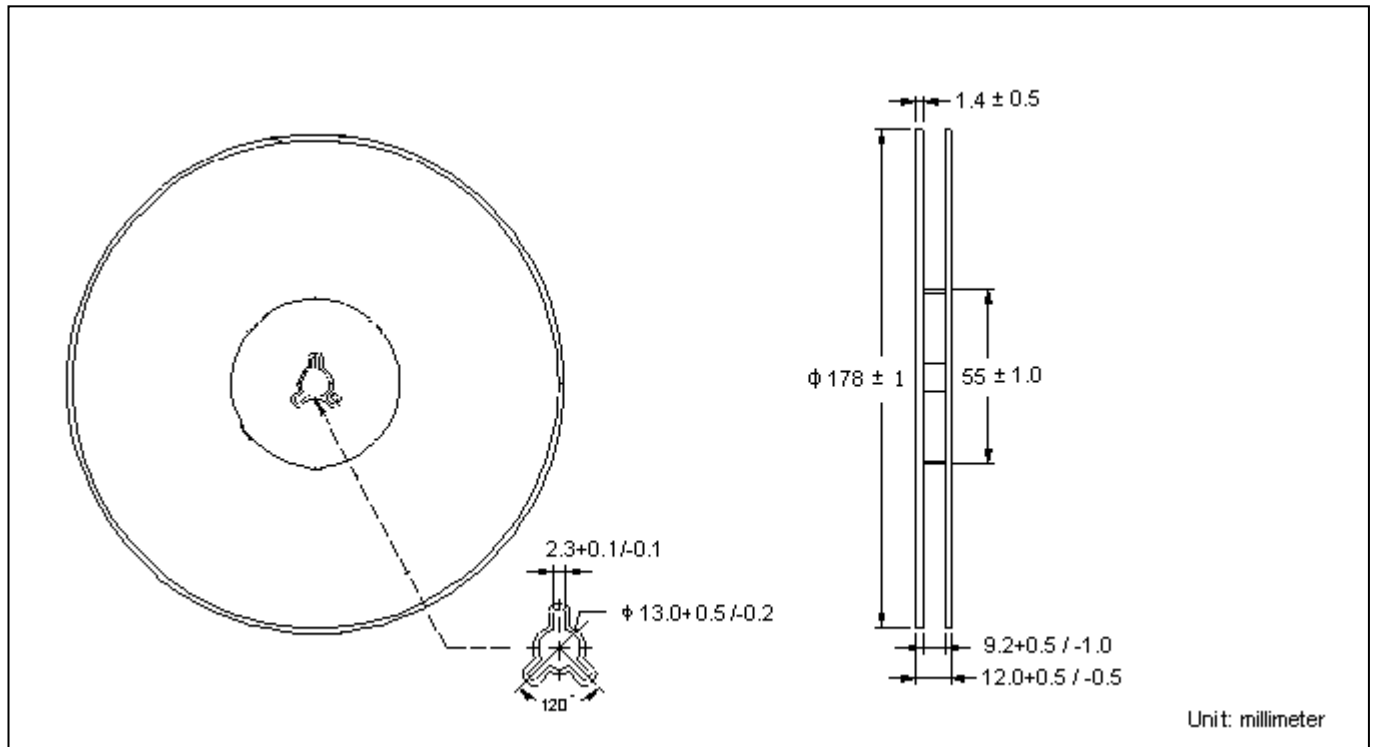
Parameter	Symbol	Limits	Unit
Supply Voltage	V <sub>CC</sub>	-50	V
Input Voltage	V <sub>IN</sub>	-40~+15	V
Output Current	I <sub>O</sub>	-30	mA
	I <sub>O(max.)</sub>	-100	mA
Power Dissipation	P <sub>d</sub>	200	mW
Junction Temperature Range	T <sub>j</sub>	-55~+150	°C
Storage Temperature Range	T <sub>stg</sub>	-55~+150	°C

**Electrical Characteristics (Ta=25°C)**

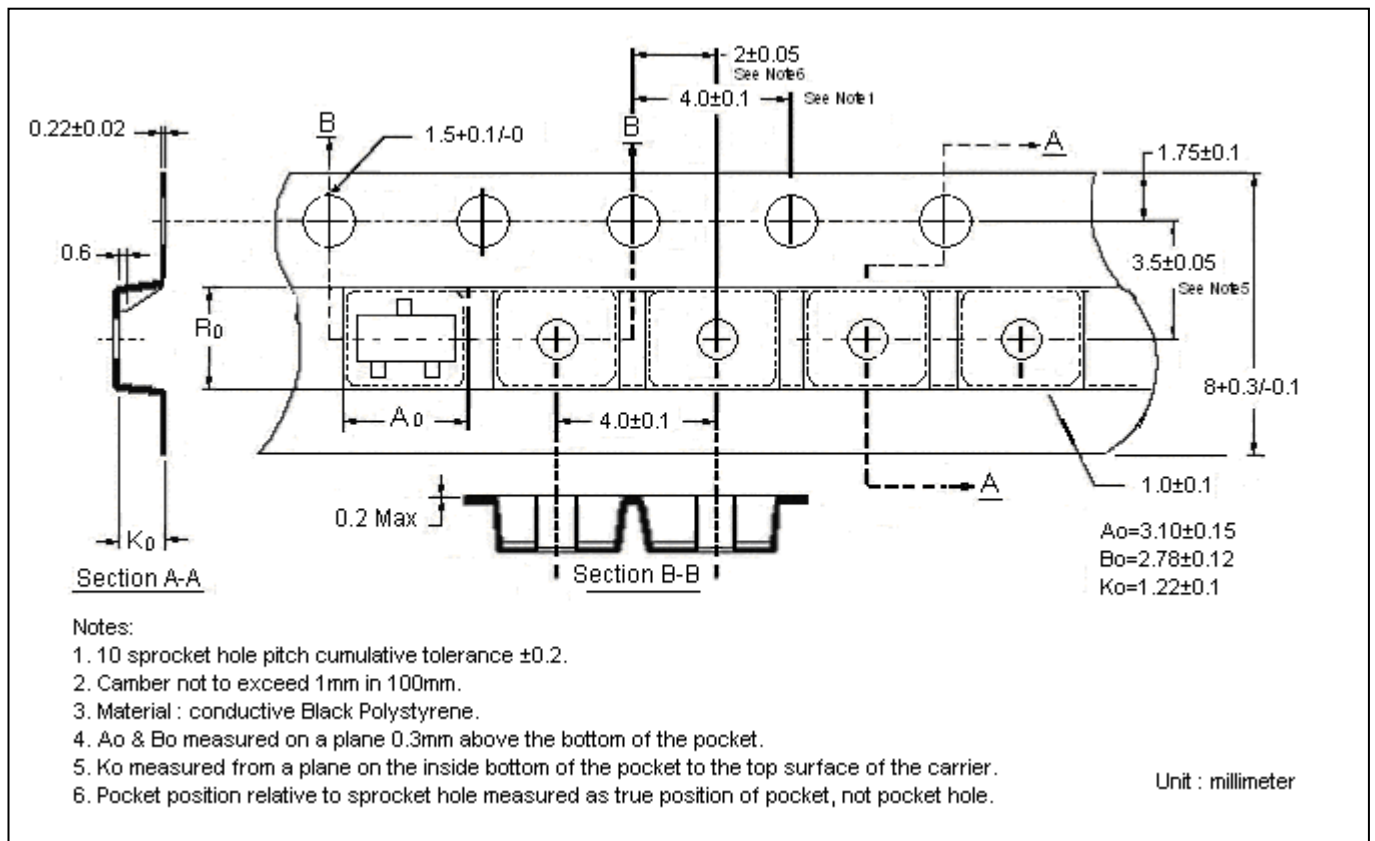
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input Voltage	V <sub>I(off)</sub>	-	-	-1	V	V <sub>CC</sub> =-5V, I <sub>O</sub> =-100μA
	V <sub>I(on)</sub>	-5	-	-	V	V <sub>O</sub> =-0.3V, I <sub>O</sub> =-2mA
Output Voltage	V <sub>O(on)</sub>	-	-0.1	-0.3	V	I <sub>O</sub> /I <sub>I</sub> =-10mA/-0.5mA
Input Current	I <sub>I</sub>	-	-	-0.16	mA	V <sub>I</sub> =-5V
Output Current	I <sub>O(off)</sub>	-	-	-0.5	μA	V <sub>CC</sub> =-50V, V <sub>I</sub> =0V
DC Current Gain	G <sub>I</sub>	33	-	-	-	V <sub>O</sub> =-5V, I <sub>O</sub> =-5mA
Input Resistance	R <sub>I</sub>	32.9	47	61.1	kΩ	-
Resistance Ratio	R <sub>2</sub> / R <sub>1</sub>	0.17	0.21	0.26	-	-
Transition Frequency	f <sub>T</sub>	-	250	-	MHz	V <sub>CE</sub> =-10V, I <sub>E</sub> =-5mA, f=100MHz*

\* Transition frequency of the device

### Reel Dimension



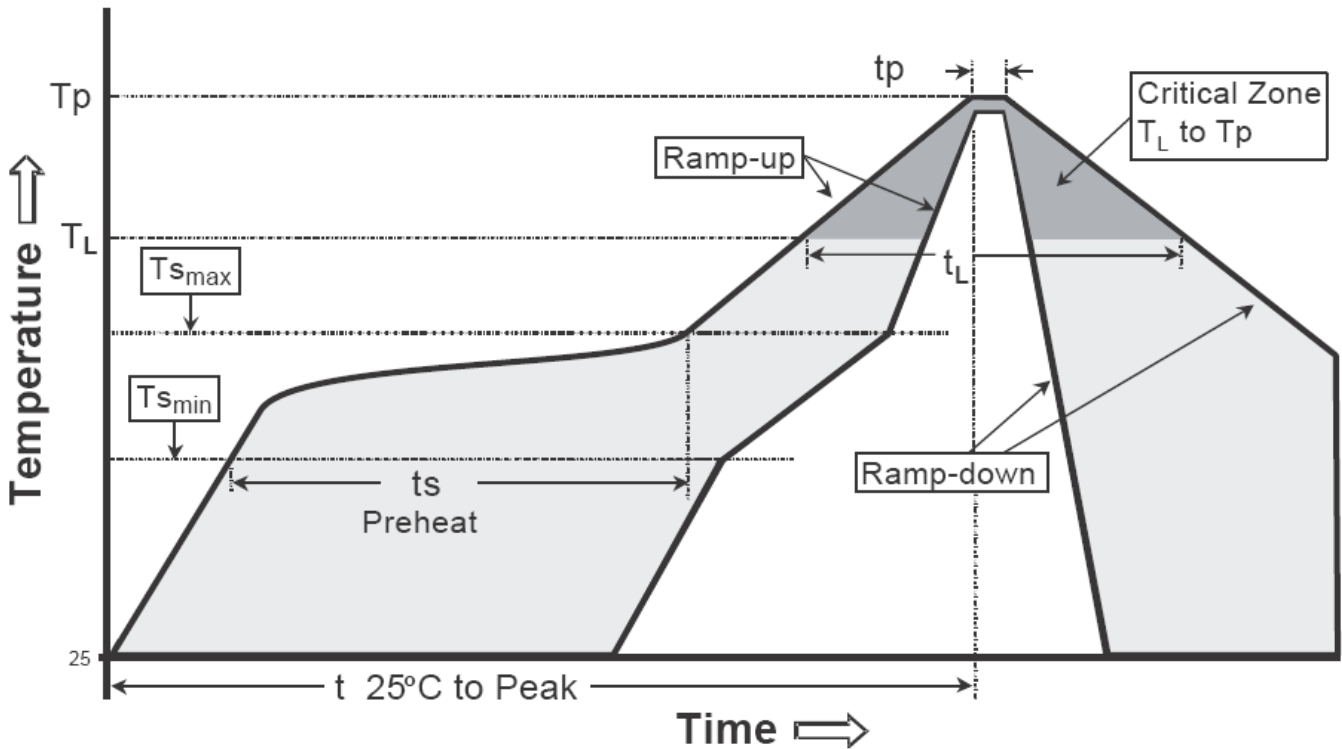
### Carrier Tape Dimension



**Recommended wave soldering condition**

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

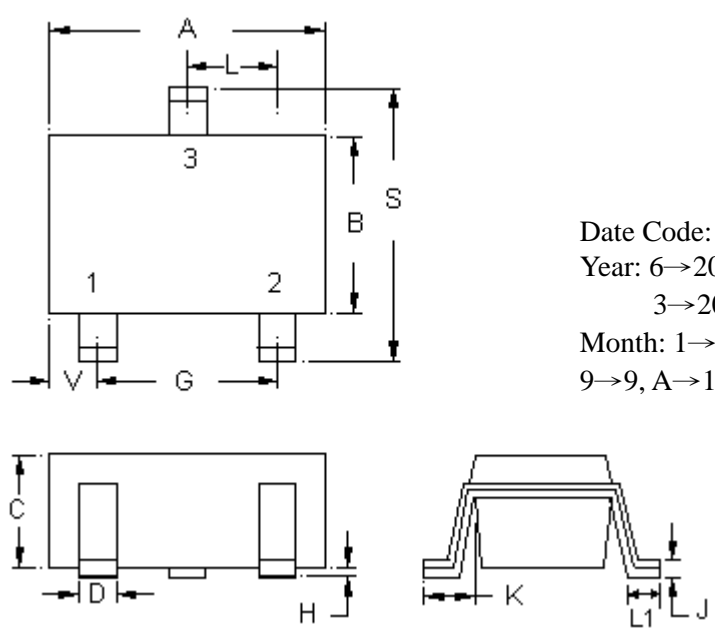
**Recommended temperature profile for IR reflow**



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (Tl)	183°C	217°C
- Time (tl)	60-150 seconds	60-150 seconds
Peak Temperature(Tp)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

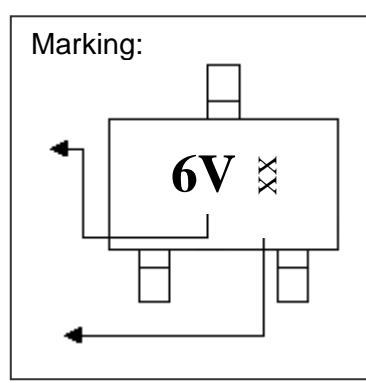
Note : All temperatures refer to topside of the package, measured on the package body surface.

**SOT-23 Dimension**



The diagram shows three views of the SOT-23 package: a top view with dimensions A, B, C, G, S, V, and L; a side view with dimensions C, D, H, and J; and a perspective view with dimensions K, L1, and L2. The top view also labels pins 1, 2, and 3.

**Marking:**



The marking diagram shows a rectangular package with a central lead and two side leads. The marking '6V XX' is shown on the top surface, with arrows pointing to the lead positions.

**Product Code**

**Date Code: Year+Month**  
 Year: 6→2021, 2→2022, 3→2023, . . . , etc  
 Month: 1→1, 2→2, . . .  
 9→9, A→10, B→11, C→12

**3-Lead SOT-23 Plastic Surface Mounted Package**  
 CYStek Package Code: N3

**Style : Pin 1.Base 2.Emitter 3.Collector**

\*:Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1102	0.1204	2.80	3.04	J	0.0032	0.0079	0.08	0.20
B	0.0472	0.0551	1.20	1.40	K	0.0118	0.0266	0.30	0.67
C	0.0335	0.0512	0.89	1.30	L	0.0335	0.0453	0.85	1.15
D	0.0118	0.0197	0.30	0.50	S	0.0830	0.1004	2.10	2.55
G	0.0669	0.0910	1.70	2.30	V	0.0098	0.0256	0.25	0.65
H	0.0000	0.0040	0.00	0.10	L1	0.0118	0.0197	0.30	0.50

- Notes :**
- 1.Controlling dimension : millimeters.
  - 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
  - 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

**Material :**

- Lead : Pure tin plated.
- Mold Compound : Epoxy resin family, flammability solid burning class:UL94V-0.

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