

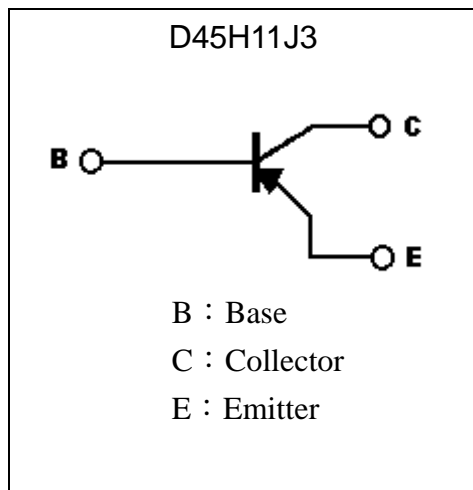
Low Vcesat PNP Epitaxial Planar Transistor

D45H11T3

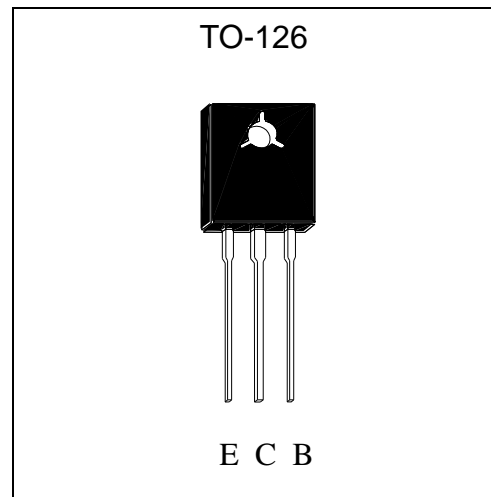
Features

- Low $V_{CE(sat)}$
- High BV_{CEO}
- Excellent current gain characteristics
- RoHS compliant package
- Pb-free lead-free and halogen-free package

Symbol

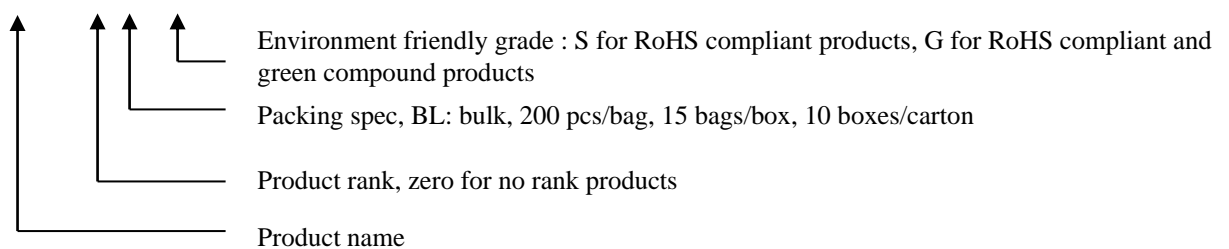


Outline



Ordering Information

Device	Package	Shipping
D45H11T3-0-BL-G	TO-126 (Pb-free lead plating package)	200 pcs / bag, 3,000 pcs/box 30,000 pcs/carton





Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V _{CBO}	-80	V
Collector-Emitter Voltage	V _{CEO}	-80	V
Emitter-Base Voltage	V _{EBO}	-5	V
Collector Current (DC)	I _C	-8	A
Collector Current (Pulse)	I _{CP}	-16 (Note 1)	
Power Dissipation @ T _A =25°C	P _D	1.75 (Note 2)	W
Power Dissipation @ T _C =25°C	P _D	20	
Thermal Resistance, Junction to Ambient	R _{θJA}	71.4 (Note 2)	°C/W
Thermal Resistance, Junction to Case	R _{θJC}	6.25	°C/W
Junction Temperature	T _J	150	°C
Storage Temperature	T _{stg}	-55~+150	°C

Note : 1. Single Pulse , Pw ≤ 380μs, Duty ≤ 2%.
 2. When mounted on a PCB with the minimum pad size.

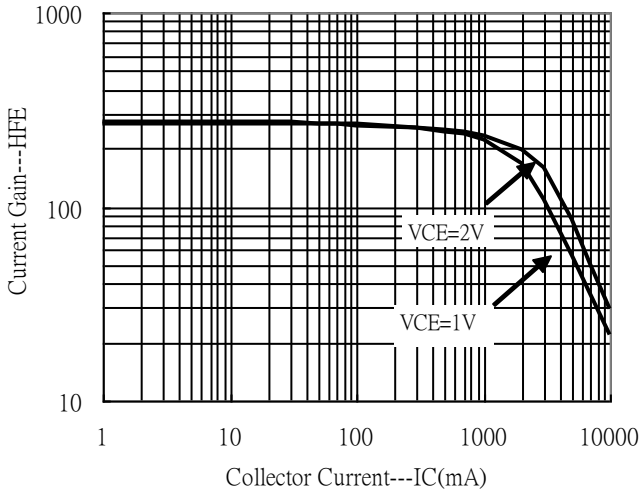
Characteristics (Ta=25°C)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV _{CEO(SUS)}	-80	-	-	V	I _C =-30mA, I _B =0
I _{CEO}	-	-	-10	μA	V _{CE} =-80V, I _B =0
I _{CES}	-	-	-10	μA	V _{CE} =-80V, V _{BE} =0
I _{EBO}	-	-	-50	μA	V _{EB} =-5V, I _C =0
*V _{CE(sat)}	-	-0.6	-1.0	V	I _C =-8A, I _B =-0.4A
*V _{BE(sat)}	-	-1.0	-1.5	V	I _C =-8A, I _B =-0.8A
*h _{FE}	60	-	-	-	V _{CE} =-1V, I _C =-2A
*h _{FE}	40	-	-	-	V _{CE} =-1V, I _C =-4A
f _T	-	40	-	MHz	V _{CE} =-10V, I _C =-500mA, f=20MHz
C _{ob}	-	230	-	pF	V _{CB} =-10V, f=1MHz
ton	-	135	-	ns	I _C =-5A, I _{B1} =-I _{B2} =-0.5A
tstg	-	500	-	ns	
tf	-	100	-	ns	

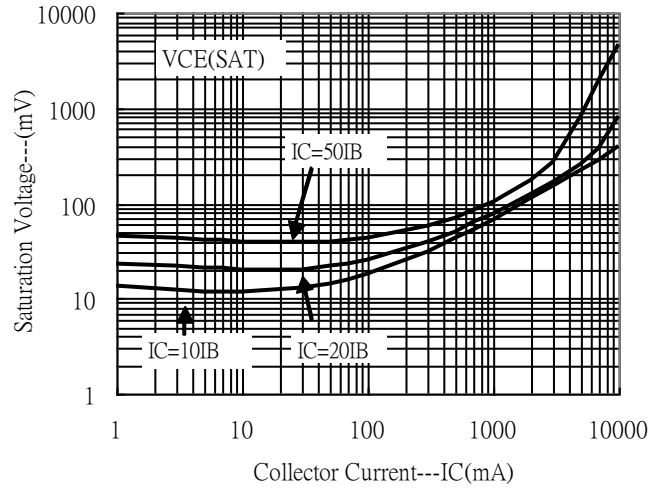
*Pulse Test : Pulse Width ≤ 380μs, Duty Cycle ≤ 2%

Typical Characteristics

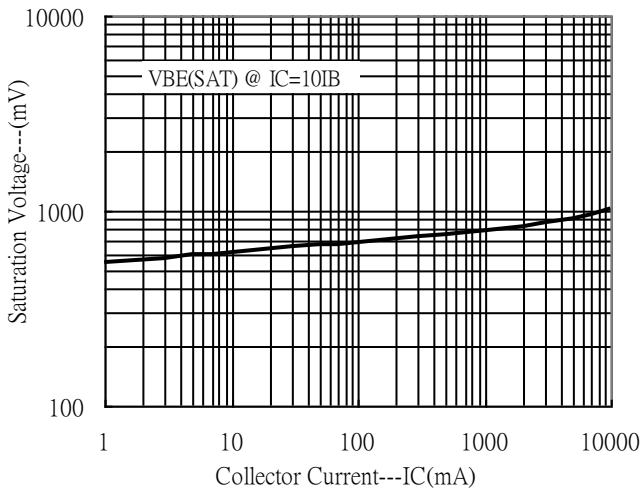
Current Gain vs Collector Current



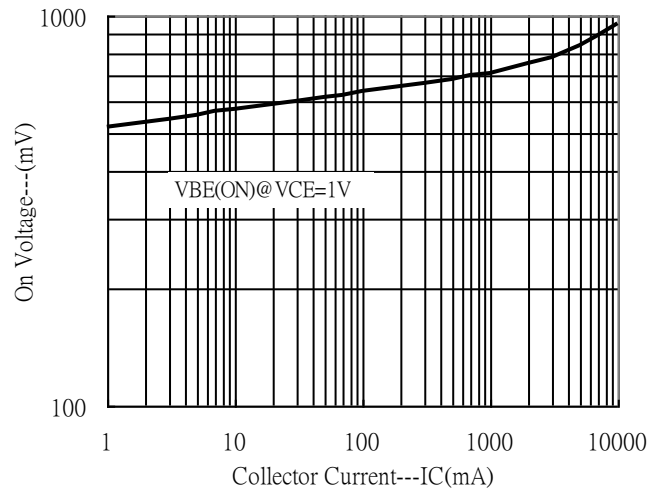
Saturation Voltage vs Collector Current



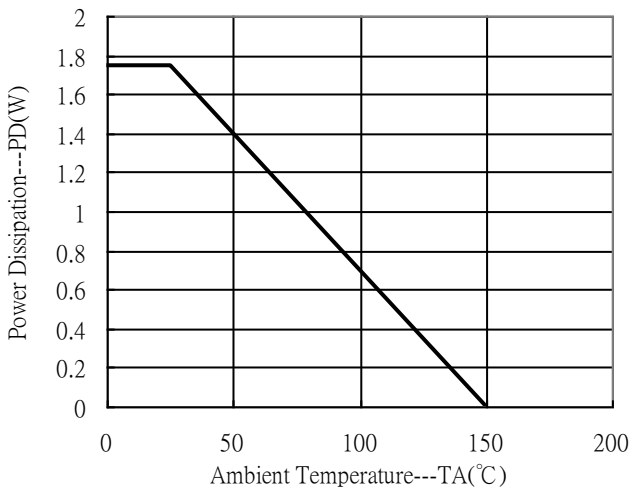
Saturation Voltage vs Collector Current



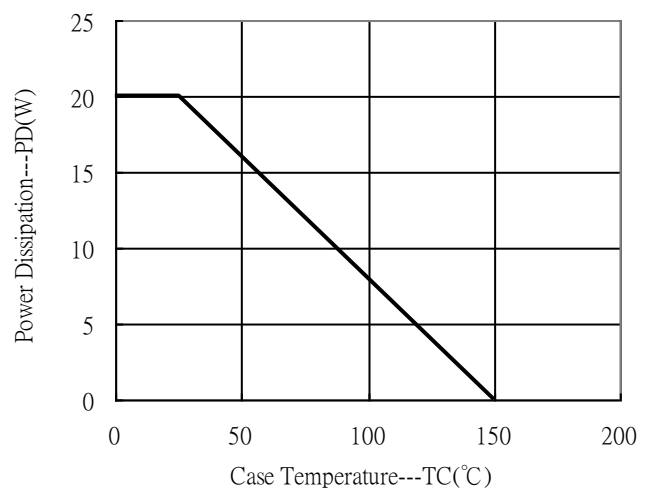
On Voltage vs Collector Current



Power Derating Curve



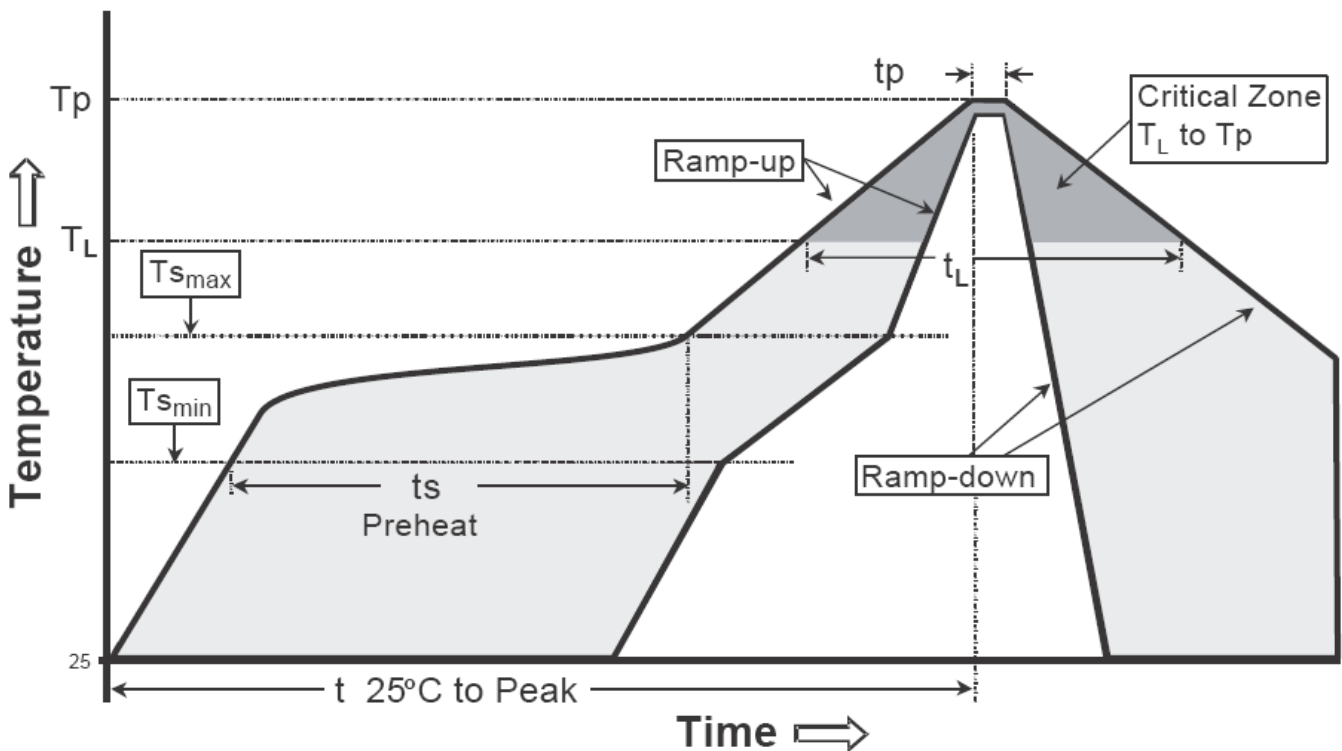
Power Derating Curve



Recommended wave soldering condition

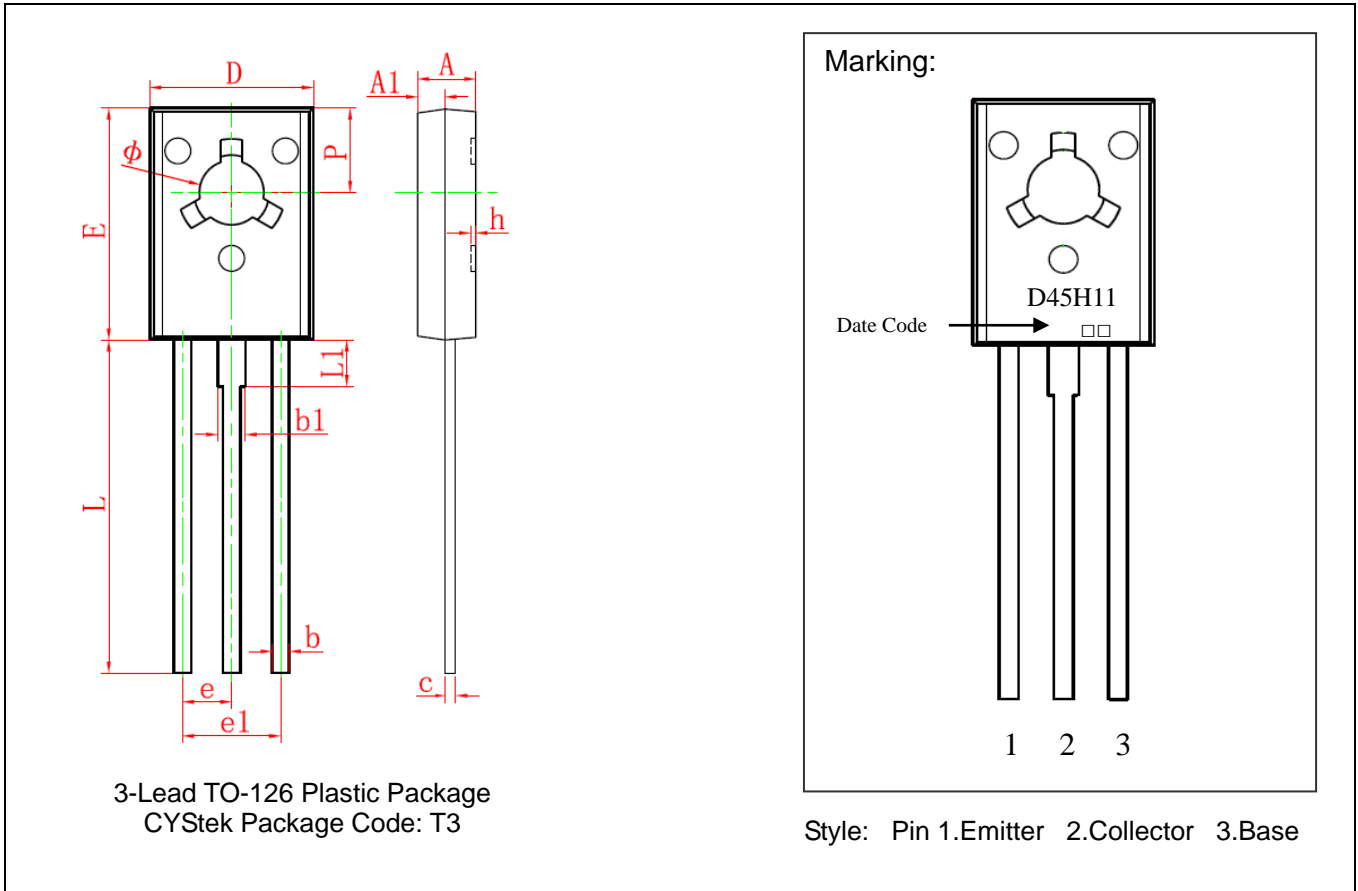
Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _p)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(t _p)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

TO-126 Dimension



3-Lead TO-126 Plastic Package
 CYStek Package Code: T3

Marking:

Date Code → □□

D45H11

1 2 3

Style: Pin 1. Emitter 2. Collector 3. Base

*: Typical

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	2.500	2.900	0.098	0.114	e	*2.290		*0.090	
A1	1.100	1.500	0.043	0.059	e1	4.480	4.680	0.176	0.184
b	0.660	0.860	0.026	0.034	h	0.000	0.300	0.000	0.012
b1	1.170	1.370	0.046	0.054	L	15.300	15.700	0.602	0.618
c	0.450	0.600	0.018	0.024	L1	2.100	2.300	0.083	0.091
D	7.400	7.800	0.291	0.307	P	3.900	4.100	0.154	0.161
E	10.600	11.000	0.417	0.433	Φ	3.000	3.200	0.118	0.126

- Notes:**
- Controlling dimension: millimeters.
 - Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 - If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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