

# Low Vcesat NPN Epitaxial Planar Transistor

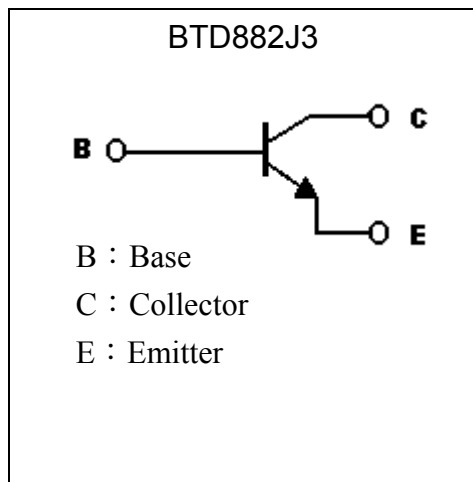
## BTD882J3

$BV_{CEO}$	50V
$I_C$	3A

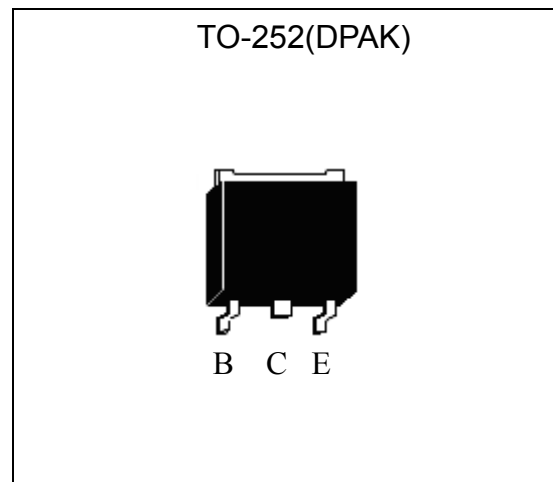
### Features

- Low  $V_{CE(sat)}$ , typically 0.25V at  $I_C / I_B = 2A / 0.2A$
- Excellent current gain characteristics
- Complementary to BTB772J3
- Pb-free lead plating and halogen-free package

### Symbol

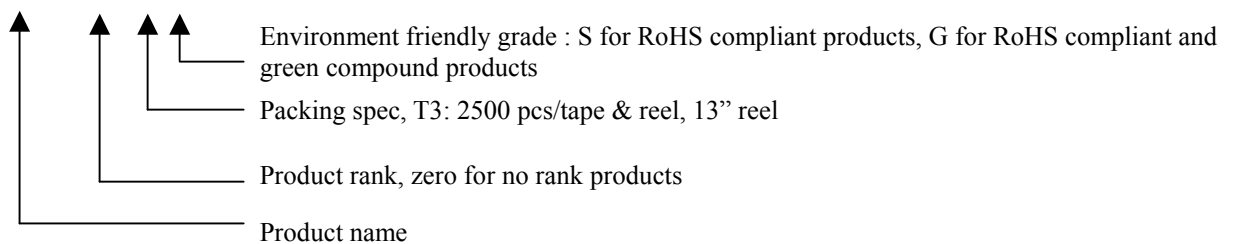


### Outline



### Ordering Information

Device	Package	Shipping
BTD882J3-X-T3-G	TO-252 (Pb-free lead plating package)	2500 pcs / tape & reel





**Absolute Maximum Ratings** (Ta=25°C)

Parameter	Symbol	Limit	Unit
Collector-Base Voltage	V <sub>CBO</sub>	50	V
Collector-Emitter Voltage	V <sub>CEO</sub>	50	V
Emitter-Base Voltage	V <sub>EBO</sub>	5	V
Collector Current	I <sub>C</sub> (DC)	3	A
	I <sub>C</sub> (Pulse)	7 *1	A
Power Dissipation	Pd(Ta=25°C)	1	W
	Pd(Tc=25°C)	10	
Junction Temperature	T <sub>j</sub>	150	°C
Storage Temperature	T <sub>stg</sub>	-55~+150	°C

Note : \*1. Single Pulse Pw ≤ 350us, Duty ≤ 2%.

**Thermal Performance**

Parameter	Symbol	Limit	Unit
Thermal Resistance, Junction-to-Ambient, max	R <sub>θJA</sub>	125	°C/W
Thermal Resistance, Junction-to-Case, max	R <sub>θJC</sub>	12.5	

**Characteristics** (Ta=25°C)

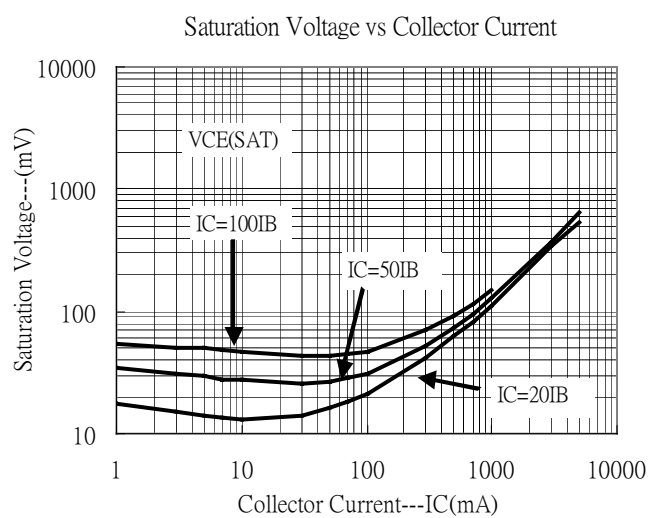
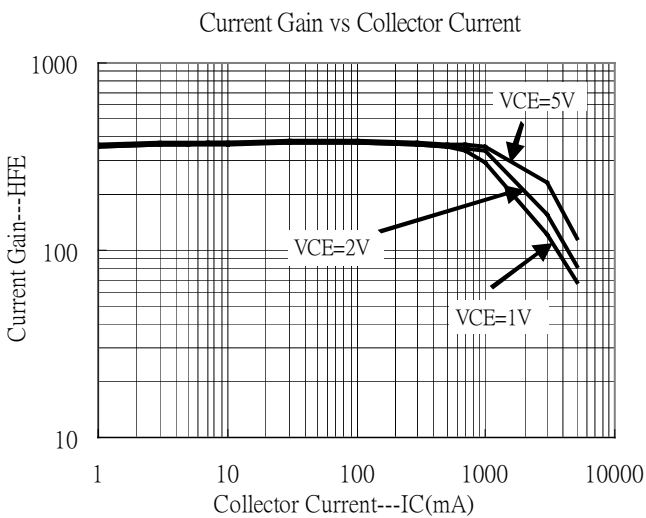
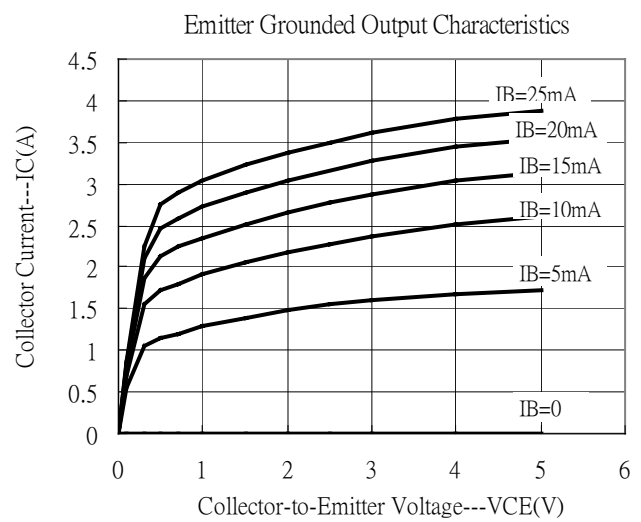
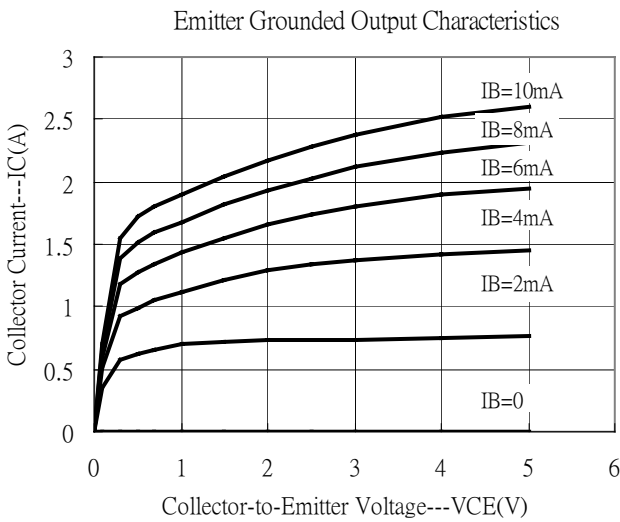
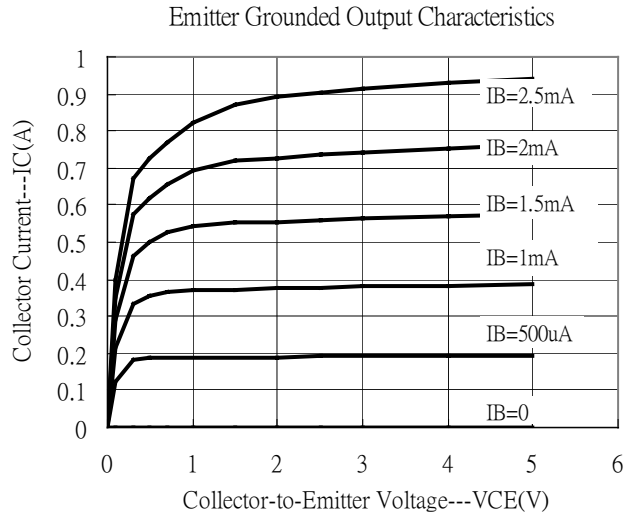
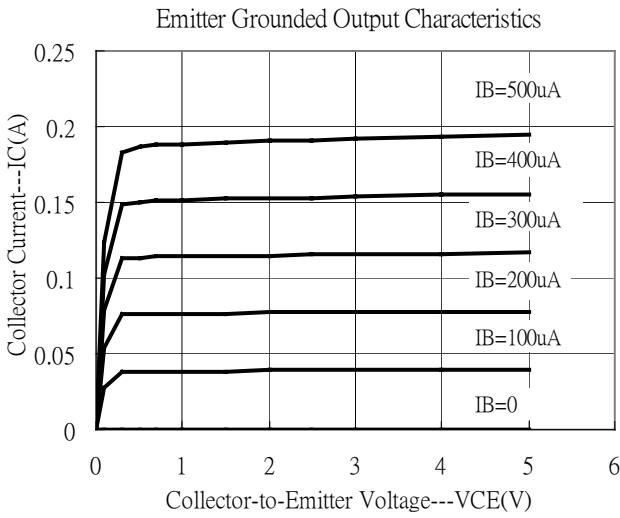
Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV <sub>CBO</sub>	50	-	-	V	I <sub>C</sub> =50μA, I <sub>E</sub> =0
BV <sub>CEO</sub>	50	-	-	V	I <sub>C</sub> =1mA, I <sub>B</sub> =0
BV <sub>EBO</sub>	5	-	-	V	I <sub>E</sub> =50μA, I <sub>C</sub> =0
I <sub>CBO</sub>	-	-	1	μA	V <sub>CB</sub> =30V, I <sub>E</sub> =0
I <sub>EBO</sub>	-	-	1	μA	V <sub>EB</sub> =3V, I <sub>C</sub> =0
*V <sub>CE(sat)</sub>	-	0.25	0.5	V	I <sub>C</sub> =2A, I <sub>B</sub> =0.2A
*V <sub>BE(sat)</sub>	-	-	2	V	I <sub>C</sub> =2A, I <sub>B</sub> =0.2A
*h <sub>FE1</sub>	150	-	-	-	V <sub>CE</sub> =2V, I <sub>C</sub> =20mA
*h <sub>FE2</sub>	180	-	560	-	V <sub>CE</sub> =2V, I <sub>C</sub> =1A
f <sub>T</sub>	-	90	-	MHz	V <sub>CE</sub> =5V, I <sub>C</sub> =0.1A, f=100MHz
Cob	-	13	-	pF	V <sub>CB</sub> =10V, f=1MHz

\*Pulse Test : Pulse Width ≤ 380μs, Duty Cycle ≤ 2%

**Classification Of h<sub>FE2</sub>**

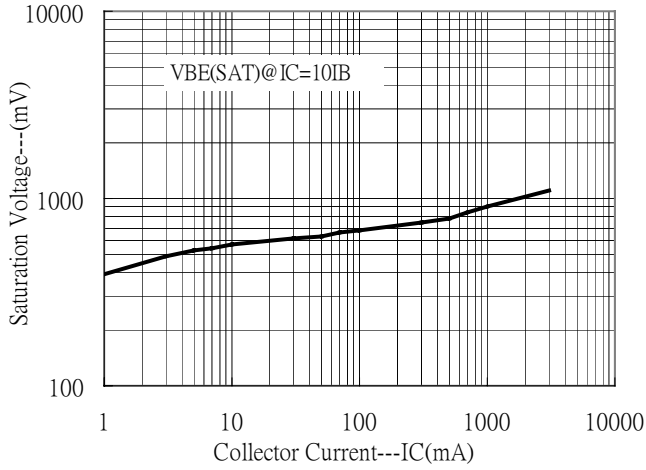
Rank	P	E
Range	180~390	270~560

**Typical Characteristics**

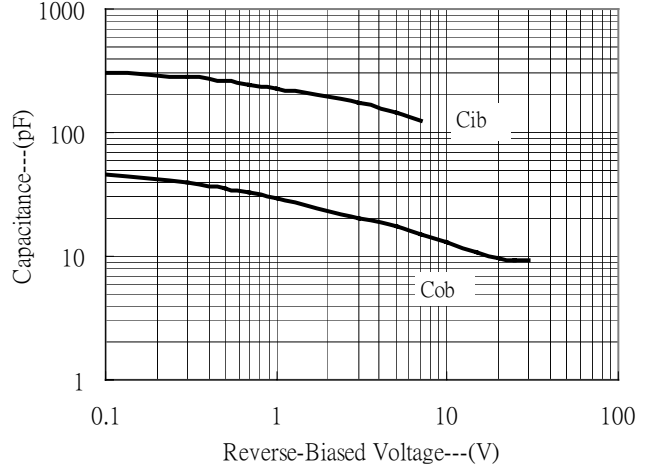


**Typical Characteristics(Cont.)**

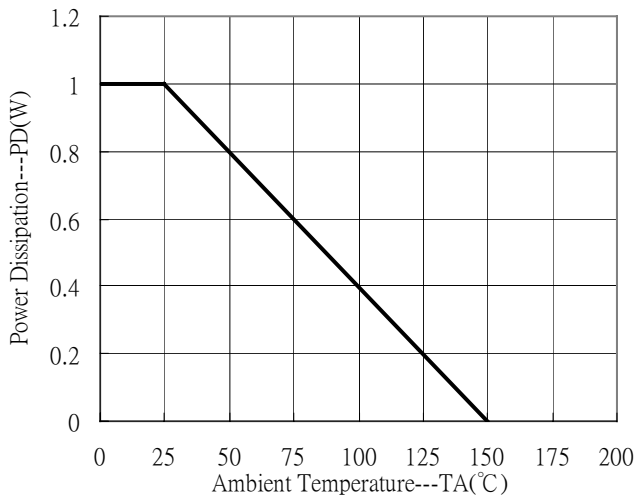
Saturation Voltage vs Collector Current



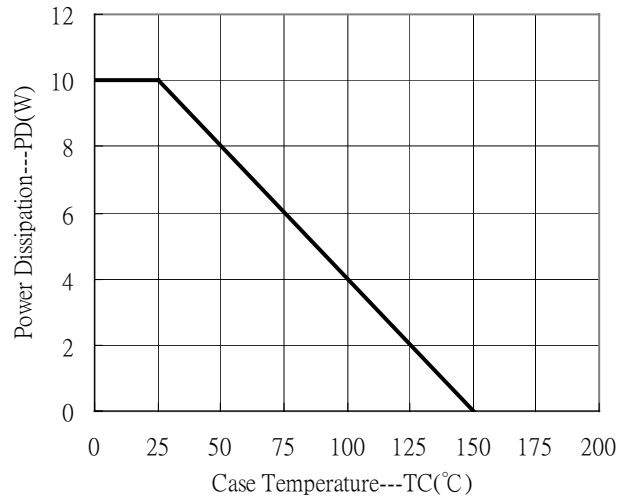
Capacitance vs Reverse-Biased Voltage



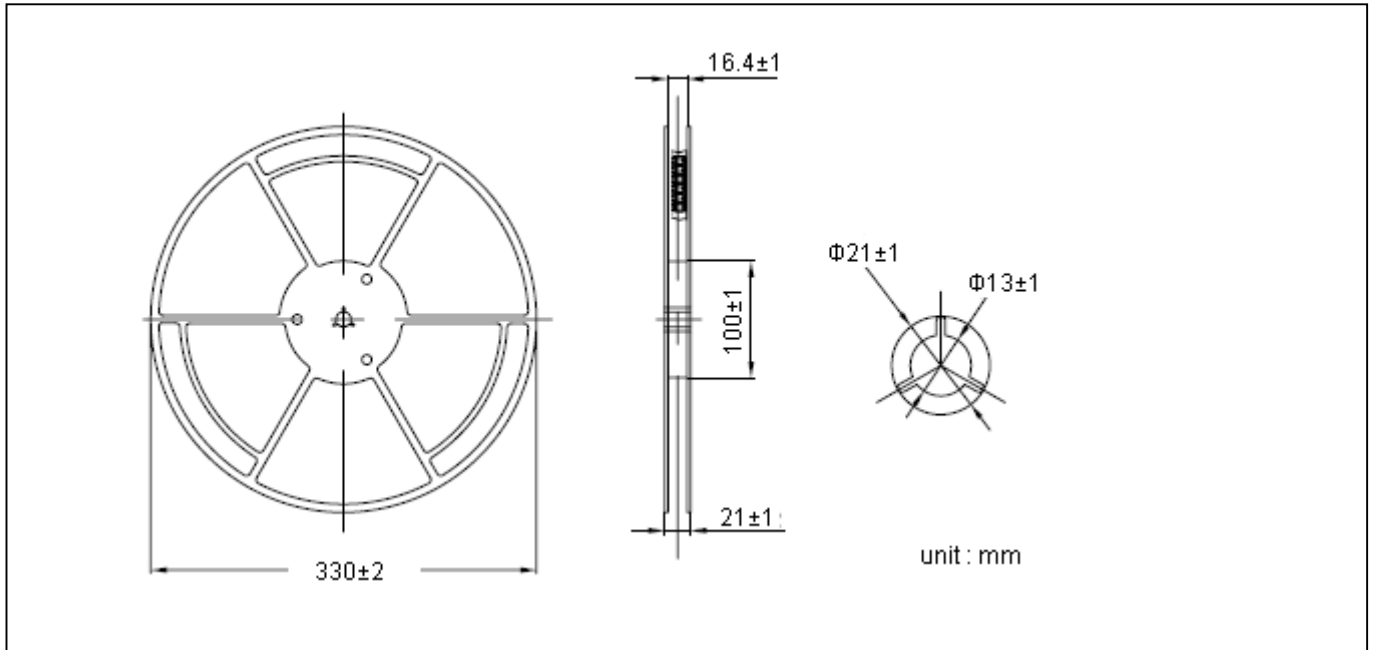
Power Derating Curve



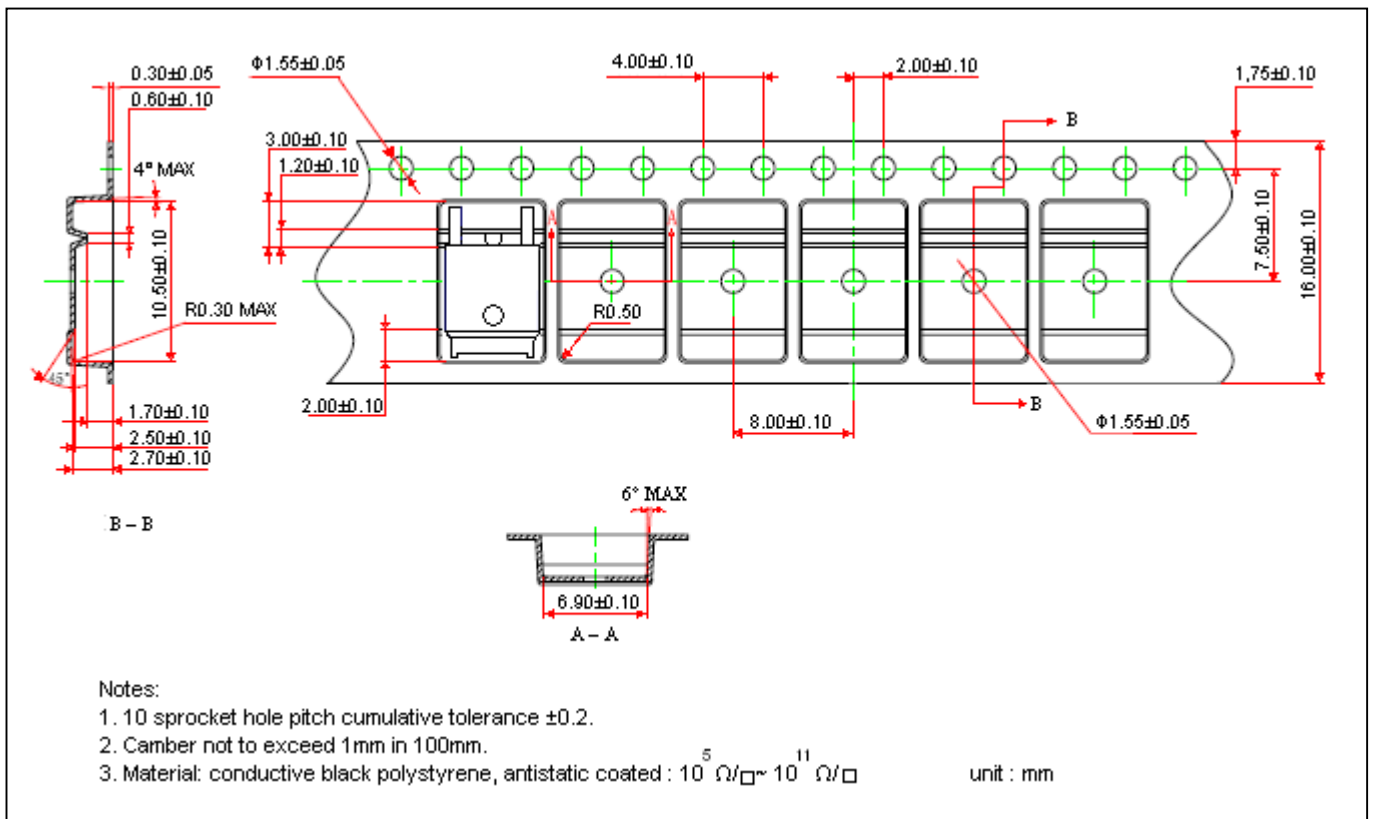
Power Derating Curve



**Reel Dimension**



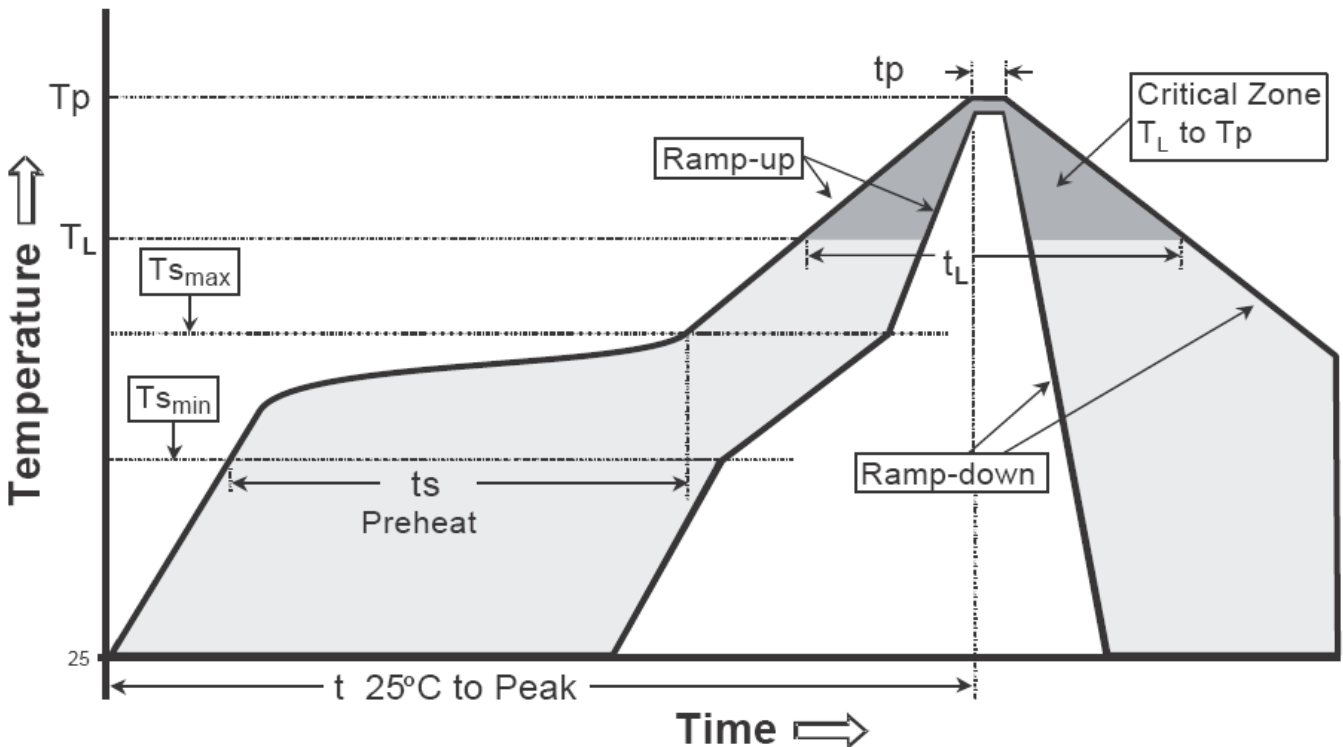
**Carrier Tape Dimension**



**Recommended wave soldering condition**

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

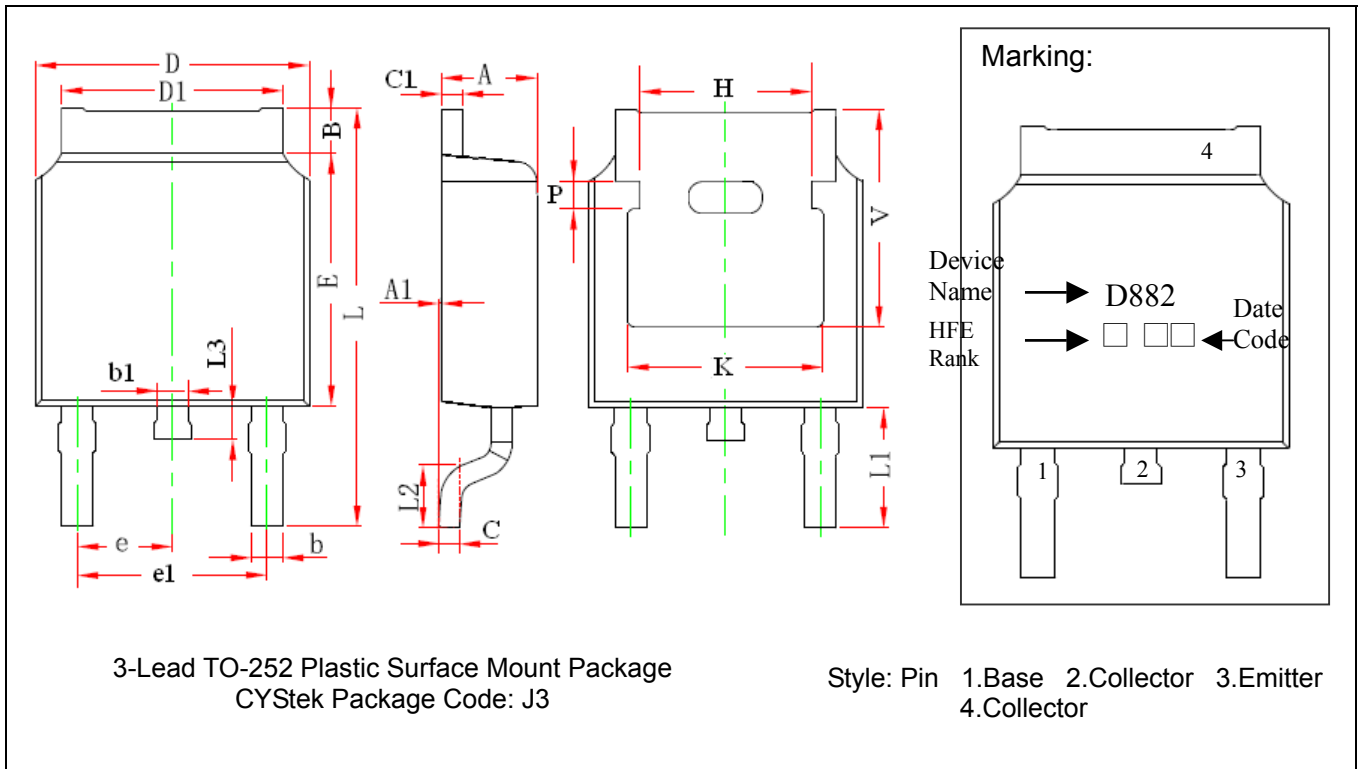
**Recommended temperature profile for IR reflow**



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T <sub>smax</sub> to T <sub>p</sub> )	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T <sub>s min</sub> )	100°C	150°C
-Temperature Max(T <sub>s max</sub> )	150°C	200°C
-Time(t <sub>s min</sub> to t <sub>s max</sub> )	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T <sub>L</sub> )	183°C	217°C
- Time (t <sub>L</sub> )	60-150 seconds	60-150 seconds
Peak Temperature(T <sub>P</sub> )	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

**TO-252 Dimension**



DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.087	0.094	2.200	2.400	e	0.086	0.094	2.186	2.386
A1	0.000	0.005	0.000	0.127	e1	0.172	0.188	4.372	4.772
B	0.039	0.048	0.990	1.210	H	0.163	REF	4.140	REF
b	0.026	0.034	0.660	0.860	K	0.190	REF	4.830	REF
b1	0.026	0.034	0.660	0.860	L	0.386	0.409	9.800	10.400
C	0.018	0.023	0.460	0.580	L1	0.114	REF	2.900	REF
C1	0.018	0.023	0.460	0.580	L2	0.055	0.067	1.400	1.700
D	0.256	0.264	6.500	6.700	L3	0.024	0.039	0.600	1.000
D1	0.201	0.215	5.100	5.460	P	0.026	REF	0.650	REF
E	0.236	0.244	6.000	6.200	V	0.211	REF	5.350	REF

**Notes:** 1.Controlling dimension: millimeters.  
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.  
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

**Material:**

- Lead : Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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