

NPN Epitaxial Planar Transistor

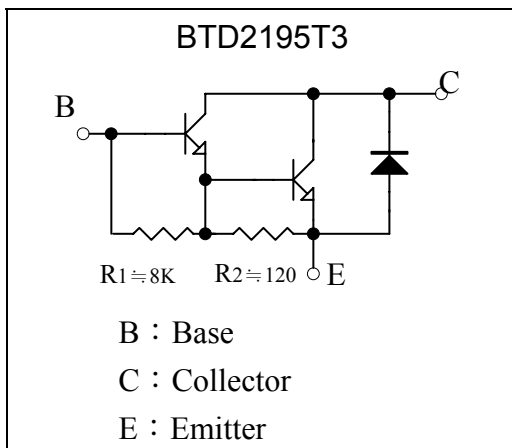
BTD2195T3

V_{CEO}	120V
I_C	4A
$V_{CE(SAT)}$	1.5V(max)

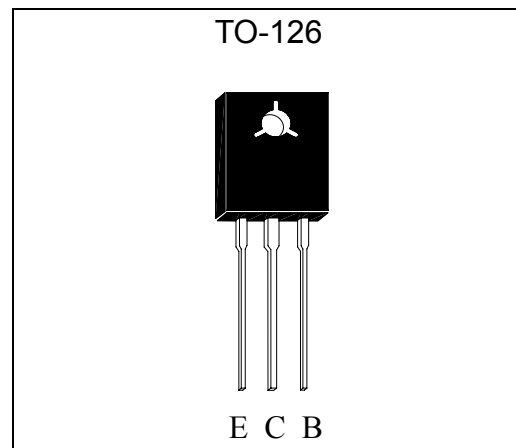
Description

The BTD2195T3 is designed for use in general purpose amplifier and low speed switching application. Pb-free lead plating package process is adopted.

Equivalent Circuit



Outline



Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit	
Collector-Base Voltage	V_{CBO}	130	V	
Collector-Emitter Voltage	V_{CEO}	120		
Emitter-Base Voltage	V_{EBO}	5		
Collector Current (DC)	I_C	4	A	
Collector Current (Pulse)	I_{CP}	6 (Note 1)		
Power Dissipation	P_D	$T_A=25^\circ C$	1.25	W
		$T_C=25^\circ C$	40	
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	100	°C/W	
Thermal Resistance, Junction to Case	$R_{\theta JC}$	3.13		
Operating Junction Temperature Range	T_j	-55~+150	°C	
Storage Temperature Range	T_{stg}	-55~+150		

Note : 1. Single Pulse $P_w \leq 300\mu s$, Duty $\leq 2\%$.



Characteristics (Ta=25°C)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV _{CEO}	120	-	-	V	I _C =1mA, I _B =0
BV _{CBO}	130	-	-	V	I _C =100μA, I _E =0
I _{CBO}	-	-	10	μA	V _{CB} =100V, I _E =0
I _{CEO}	-	-	10	μA	V _{CE} =100V, I _B =0
I _{EBO}	-	-	2	mA	V _{EB} =5V, I _C =0
*V _{CE(sat)}	-	-	1.5	V	I _C =2A, I _B =2mA
*V _{BE(on)}			2	V	V _{CE} =4V, I _C =2A
*h _{FE1}	1000	-	-	-	V _{CE} =4V, I _C =1A
*h _{FE2}	1000	-	-	-	V _{CE} =4V, I _C =2A
Cob	-		200	pF	V _{CB} =10V, I _E =0A, f=1MHz

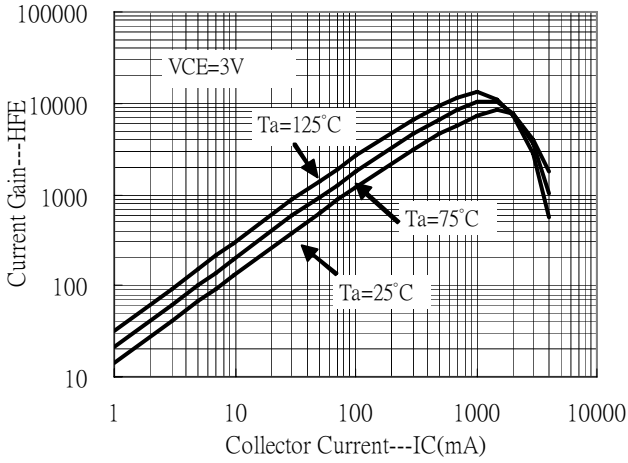
*Pulse Test : Pulse Width ≤380μs, Duty Cycle≤2%

Ordering Information

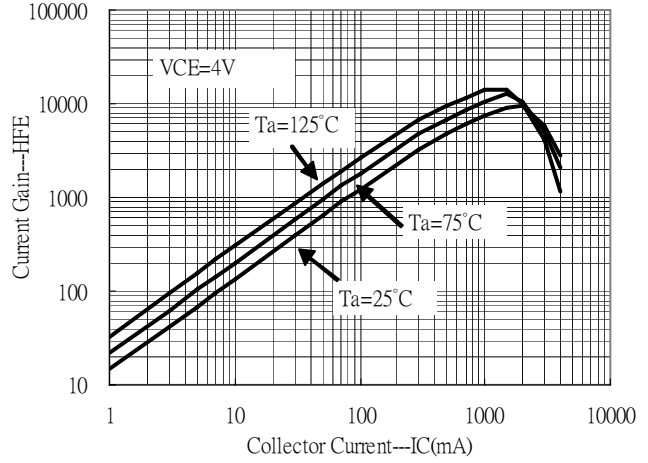
Device	Package	Shipping	Marking
BTD2195T3	TO-126 (Pb-free lead plating)	200 pcs / bag, 15 bags/box, 10 boxes/carton	D2195

Typical Characteristics

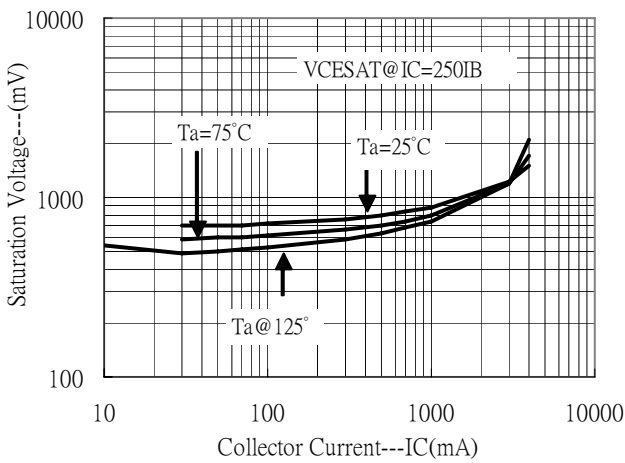
Current Gain vs Collector Current



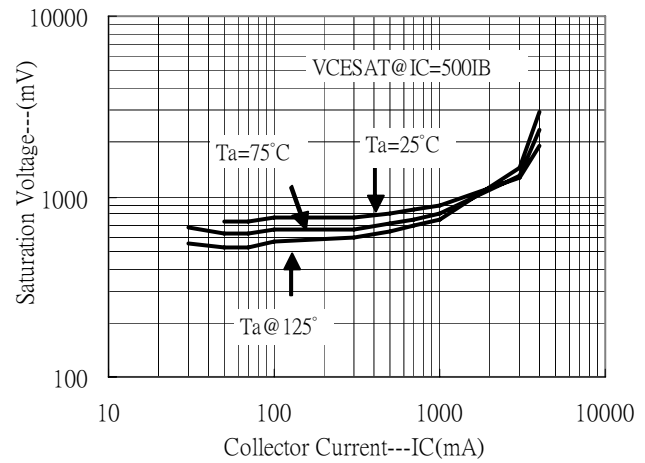
Current Gain vs Collector Current



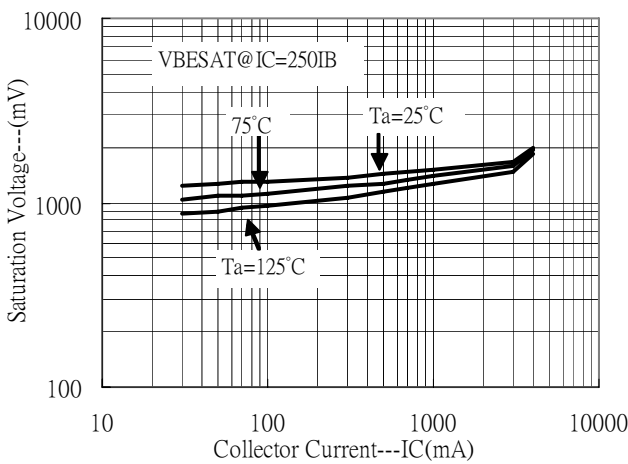
Saturation Voltage vs Collector Current



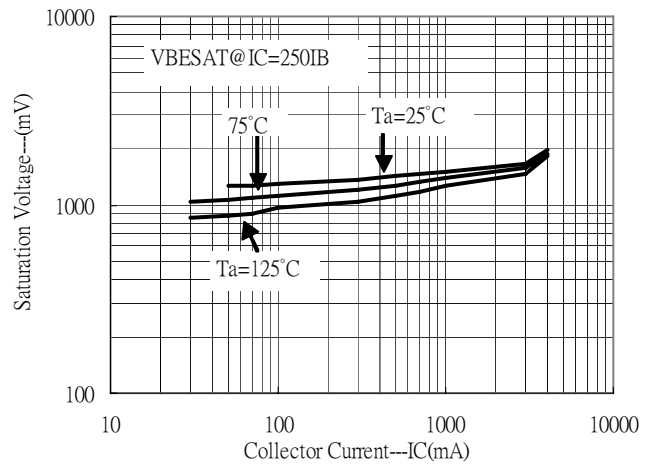
Saturation Voltage vs Collector Current



Saturation Voltage vs Collector Current

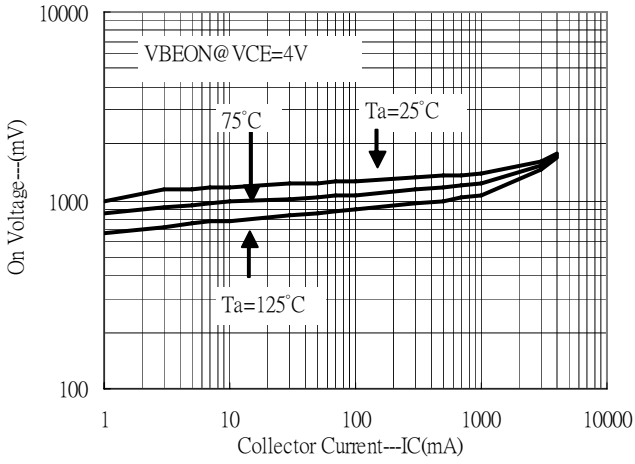


Saturation Voltage vs Collector Current

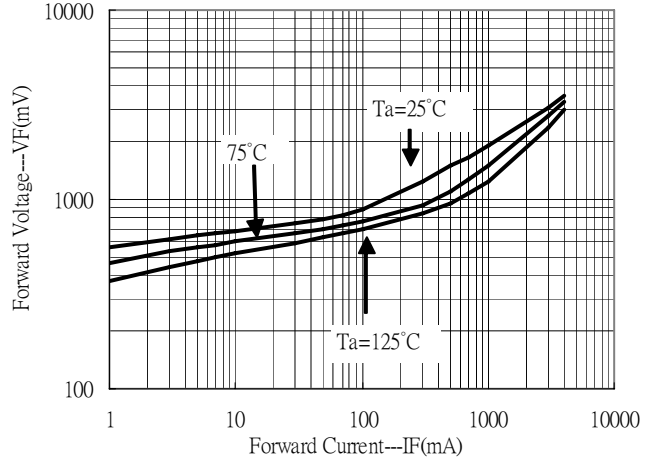


Typical Characteristics(Cont.)

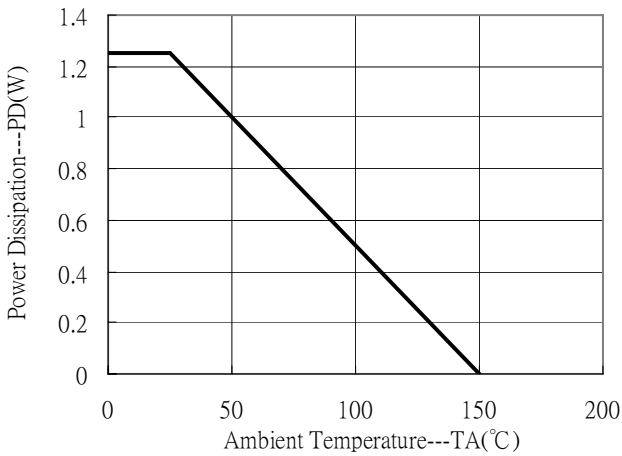
On Voltage vs Collector Current



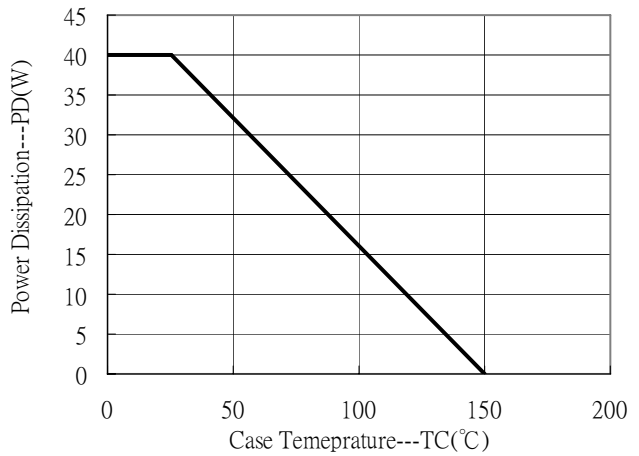
Built-in Diode Characteristics



Power Derating Curve



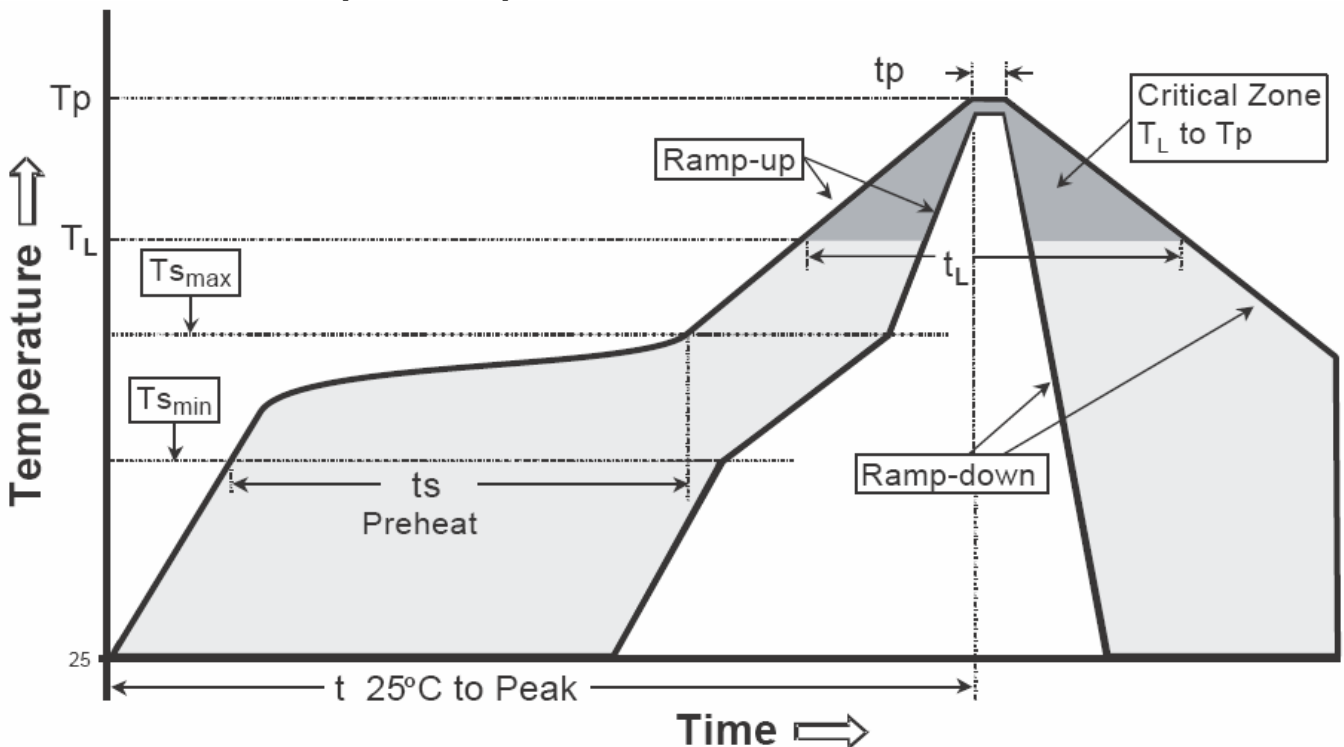
Power Derating Curve



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

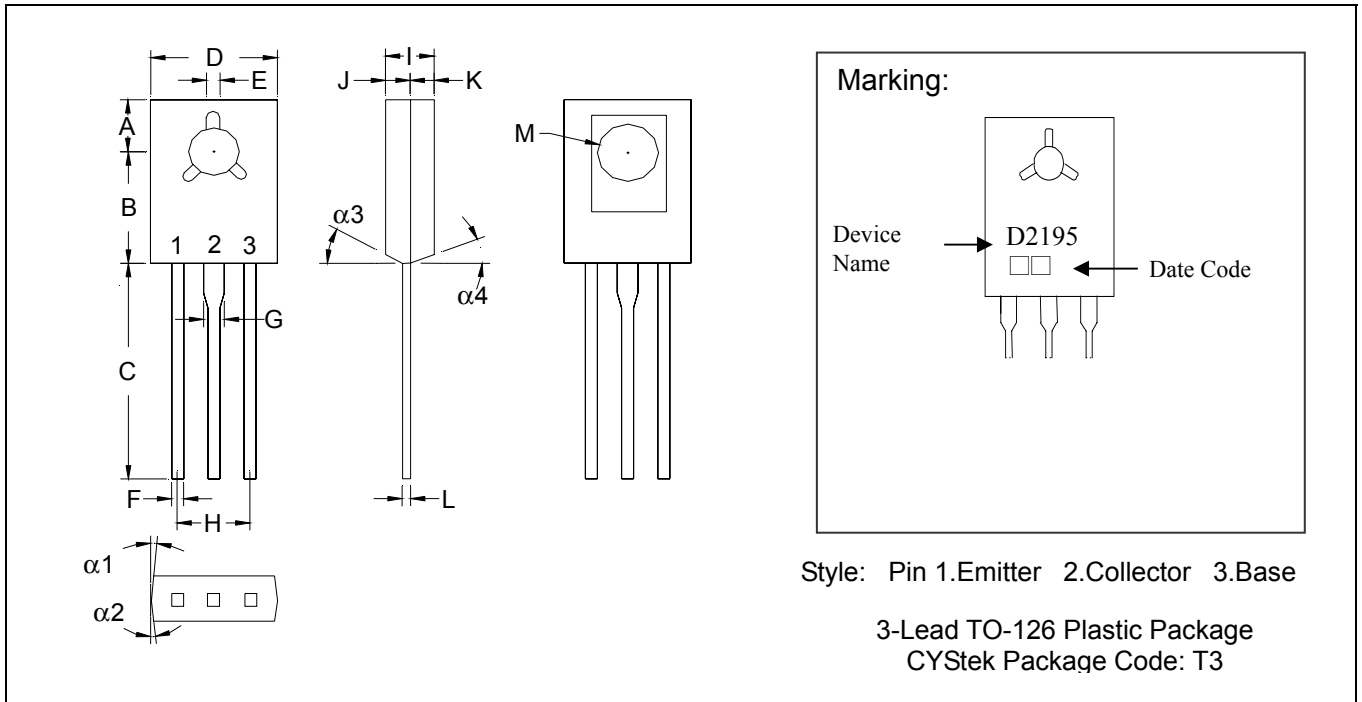
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (Tl)	183°C	217°C
- Time (tl)	60-150 seconds	60-150 seconds
Peak Temperature(Tp)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-126 Dimension



*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
$\alpha 1$	-	*3°	-	*3°	F	0.0280	0.0319	0.71	0.81
$\alpha 2$	-	*3°	-	*3°	G	0.0480	0.0520	1.22	1.32
$\alpha 3$	-	*3°	-	*3°	H	0.1709	0.1890	4.34	4.80
$\alpha 4$	-	*3°	-	*3°	I	0.0950	0.1050	2.41	2.66
A	0.1500	0.1539	3.81	3.91	J	0.0450	0.0550	1.14	1.39
B	0.2752	0.2791	6.99	7.09	K	0.0450	0.0550	1.14	1.39
C	0.5315	0.6102	13.50	15.50	L	-	*0.0217	-	*0.55
D	0.2854	0.3039	7.52	7.72	M	0.1378	0.1520	3.50	3.86
E	0.0374	0.0413	0.95	1.05					

Notes: 1. Controlling dimension: millimeters.
 2. Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3. If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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