

Low Vcesat NPN Epitaxial Planar Transistor

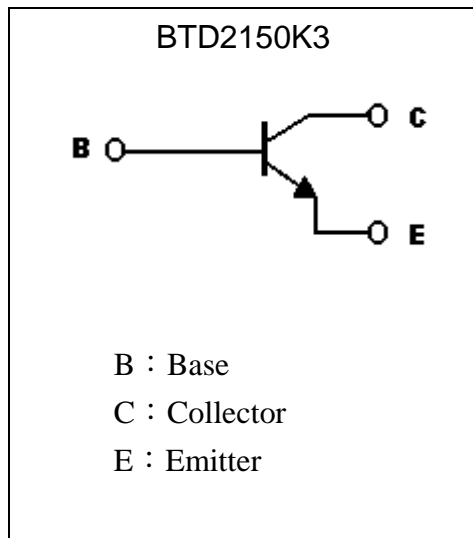
BTD2150K3

BV_{CEO}	50V
I_C	4A
$R_{CE(SAT)}$ typ.	100m Ω

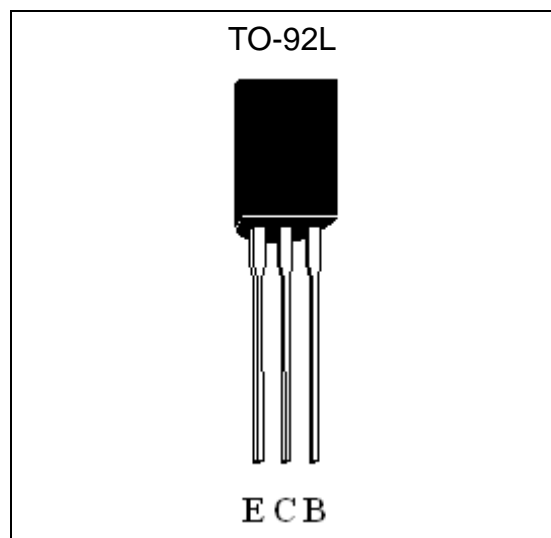
Features

- Low $V_{CE(sat)}$, $V_{CE(sat)}=0.14$ V (typical), at $I_C / I_B = 1A / 10mA$
- Excellent current gain characteristics
- Complementary to BTB1424K3
- Pb-free lead plating package

Symbol

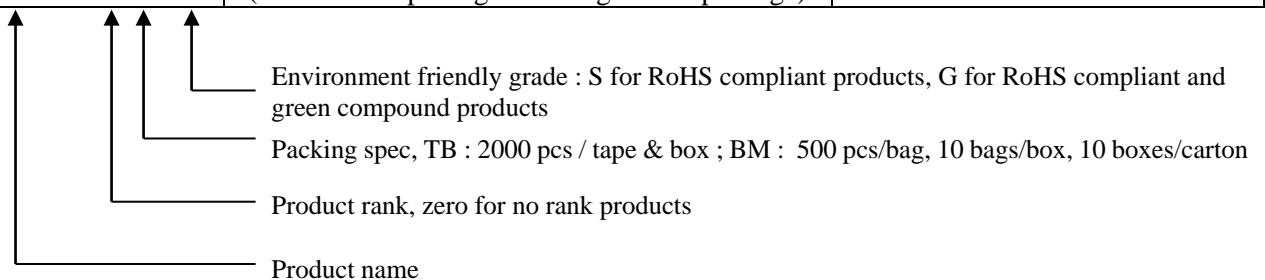


Outline



Ordering Information

Device	Package	Shipping
BTD2150K3-0-TB-G	TO-92L (Pb-free lead plating and halogen-free package)	2000 pcs / tape & box
BTD2150K3-0-BM-G	TO-92L (Pb-free lead plating and halogen-free package)	500 pcs / bag, 10 bags/box, 10 boxes/carton



**Absolute Maximum Ratings** (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V _{CBO}	80	V
Collector-Emitter Voltage	V _{CEO}	50	V
Emitter-Base Voltage	V _{EBO}	6	V
Collector Current (DC)	I _C	4	A
Collector Current (Pulse) (Note 1)	I _{CP}	7	A
Base Current	I _B	0.8	A
Power Dissipation	P _D	0.9	W
Operating Junction Temperature Range	T _j	-55~+150	°C
Storage Temperature Range	T _{stg}	-55~+150	°C

Note 1: Single pulse, Pw≤300μs, Duty Cycle≤2%.

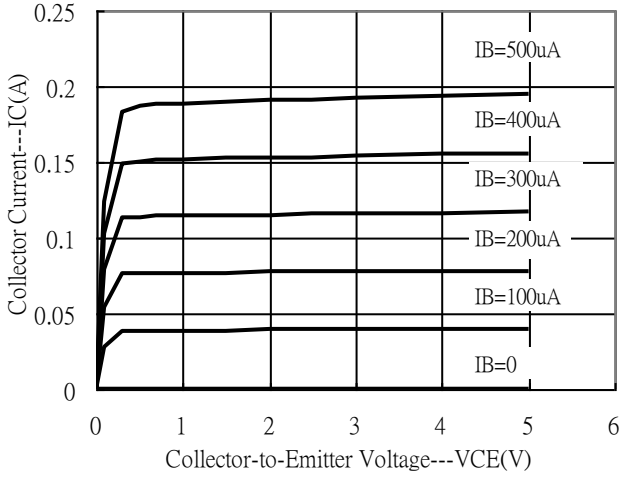
Characteristics (Ta=25°C)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV _{CBO}	80	-	-	V	I _C =50μA, I _E =0
BV _{CEO}	50	-	-	V	I _C =1mA, I _B =0
BV _{EBO}	6	-	-	V	I _E =50μA, I _C =0
I _{CBO}	-	-	0.1	μA	V _{CB} =60V, I _E =0
I _{EBO}	-	-	0.1	μA	V _{EB} =5V, I _C =0
*V _{CE(sat)}	-	0.14	0.25	V	I _C =1A, I _B =10mA
*V _{CE(sat)}	-	0.2	0.4	V	I _C =2A, I _B =0.2A
*R _{CE(sat)}	-	0.1	0.2	Ω	I _C =2A, I _B =0.2A
*V _{BE(sat)}	0.8	1	1.5	V	I _C =2A, I _B =0.2A
*h _{FE1}	250	-	-	-	V _{CE} =2V, I _C =0.1A
*h _{FE2}	270	-	560	-	V _{CE} =2V, I _C =0.5A
*h _{FE3}	200	-	-	-	V _{CE} =2V, I _C =1A
f _T	-	90	-	MHz	V _{CE} =5V, I _C =0.1A, f=100MHz
C _{ob}	-	45	-	pF	V _{CB} =10V, f=1MHz

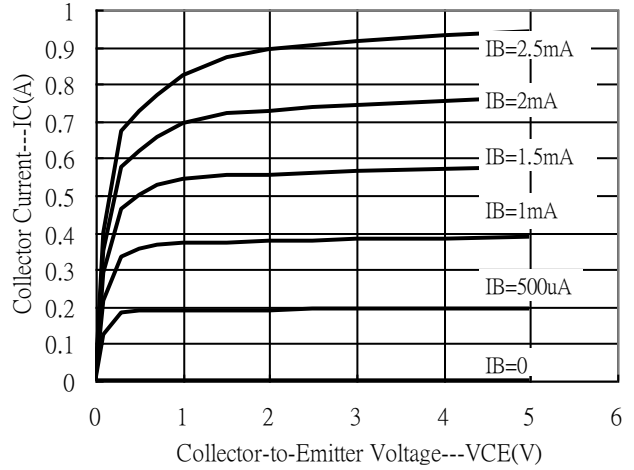
*Pulse Test : Pulse Width ≤380μs, Duty Cycle≤2%

Typical Characteristics

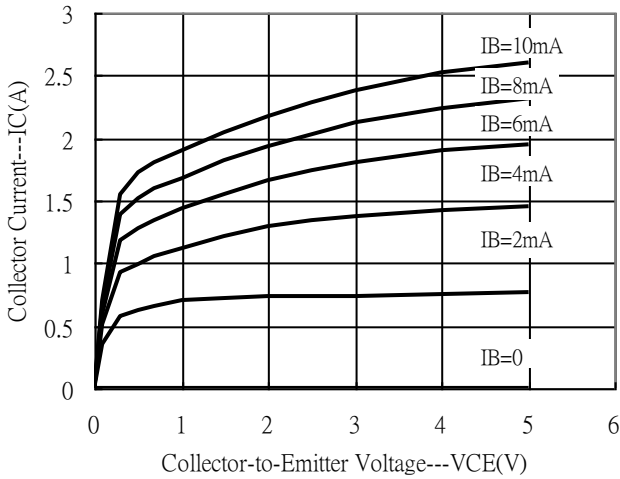
Emitter Grounded Output Characteristics



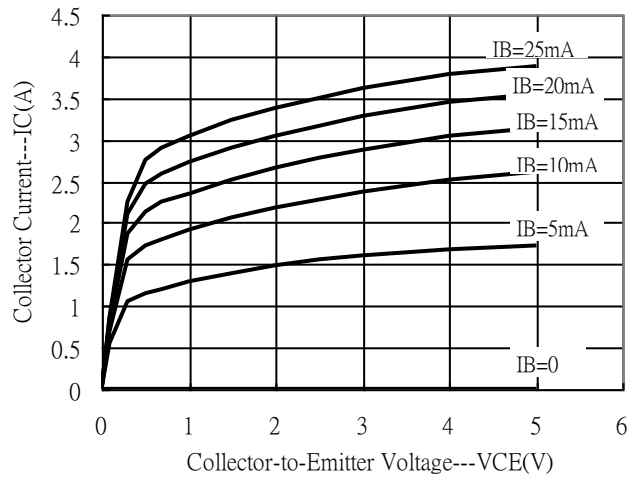
Emitter Grounded Output Characteristics



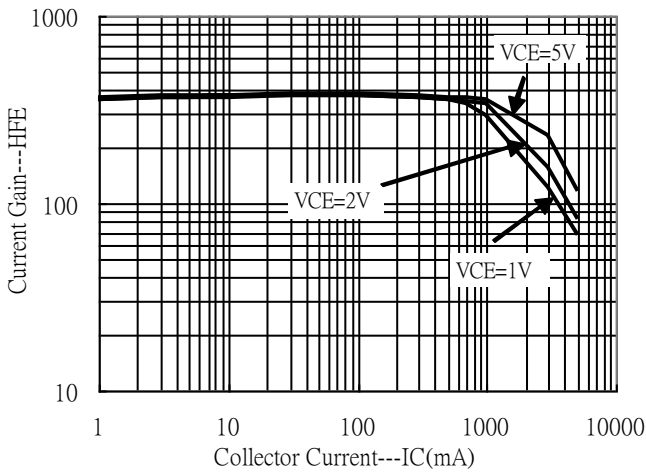
Emitter Grounded Output Characteristics



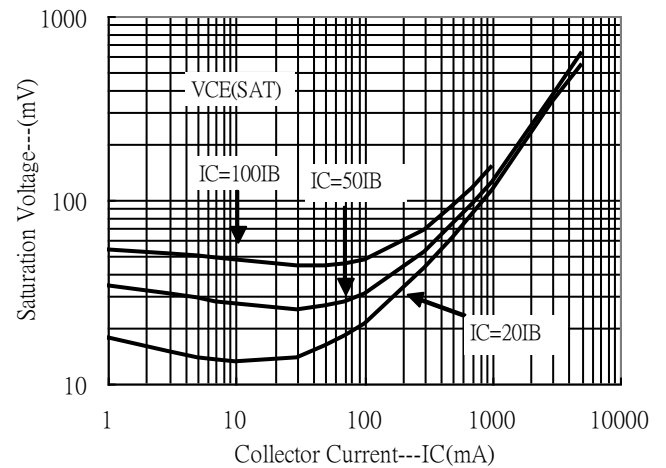
Emitter Grounded Output Characteristics



Current Gain vs Collector Current

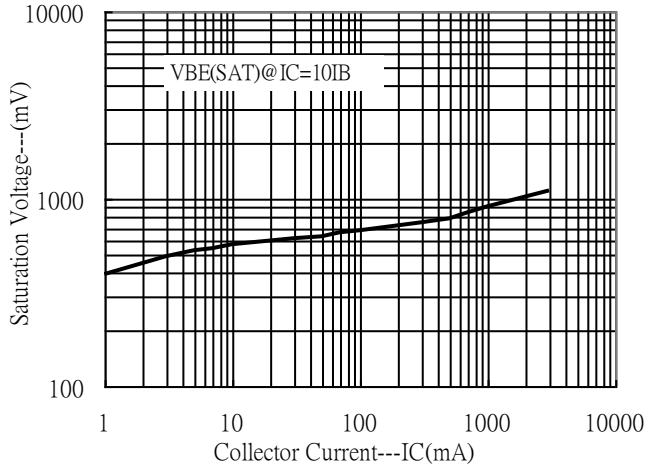


Saturation Voltage vs Collector Current

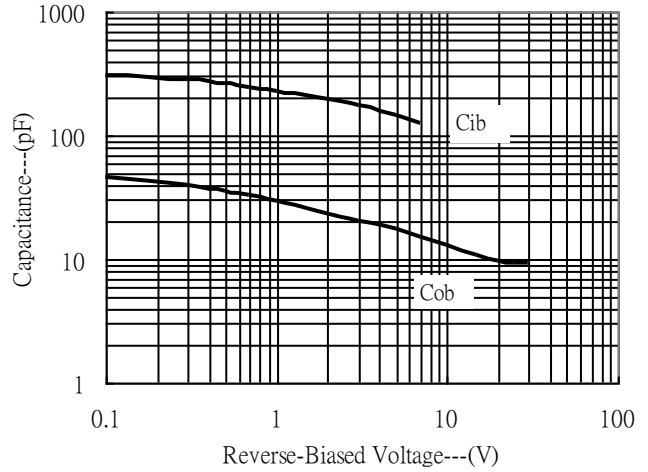


Typical Characteristics(Cont.)

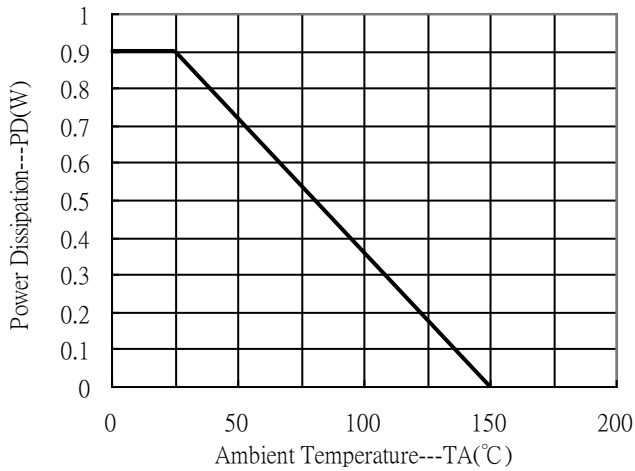
Saturation Voltage vs Collector Current



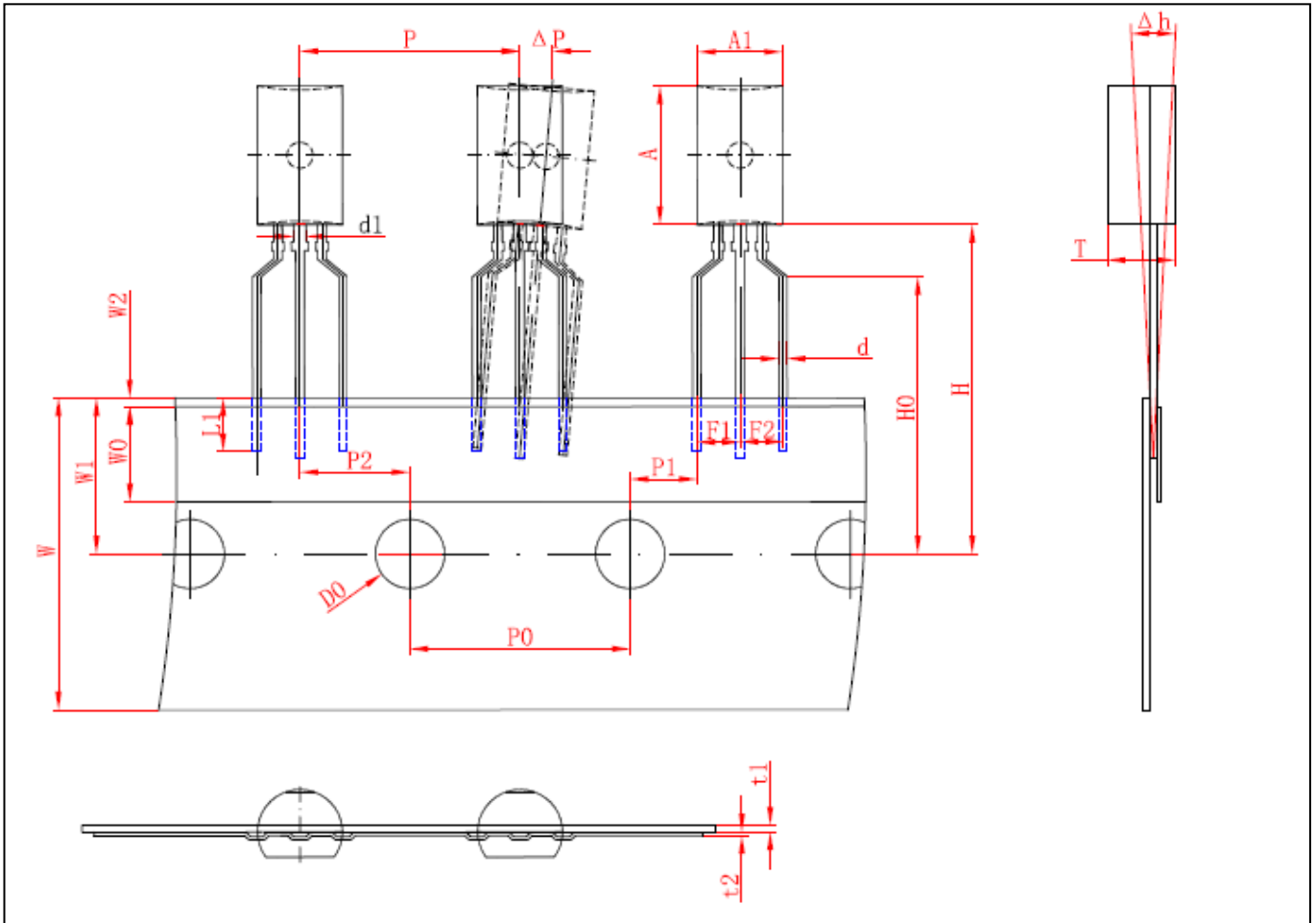
Capacitance vs Reverse-Biased Voltage



Power Derating Curve



TO-92L Taping Outline

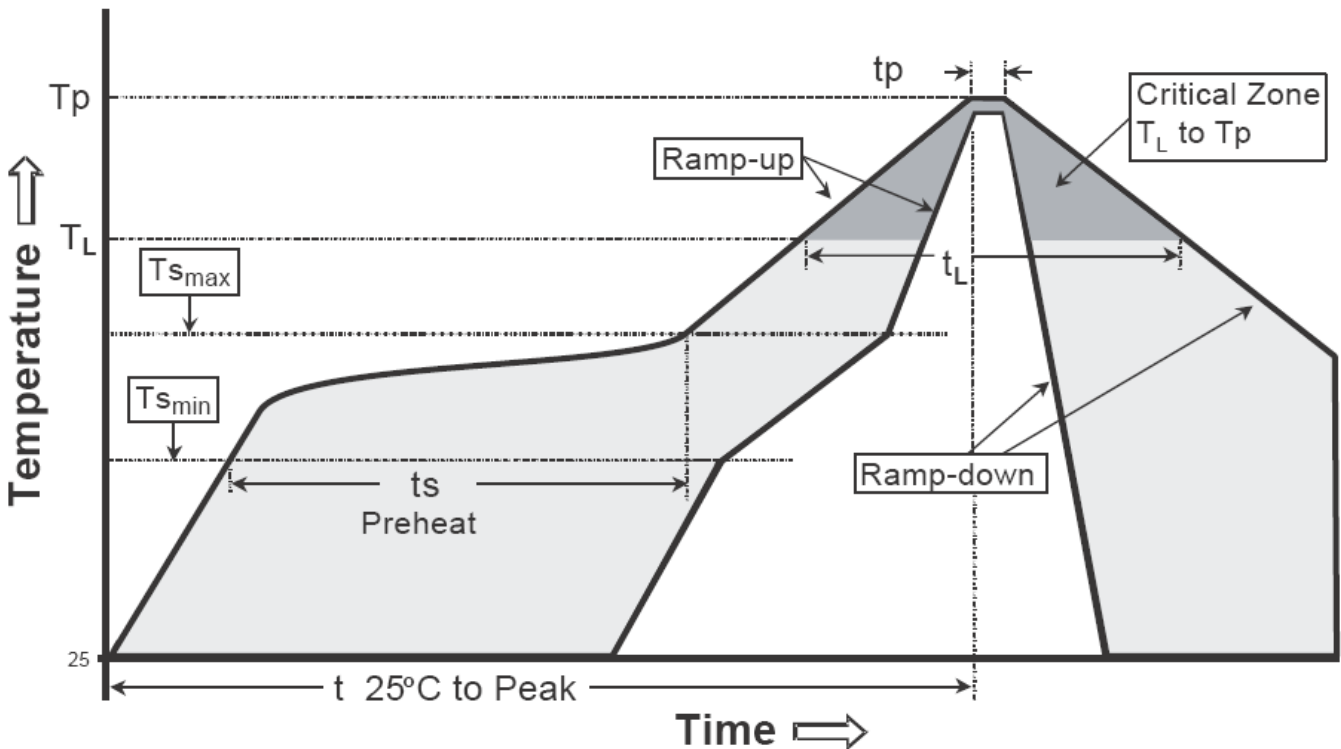


DIM	Item	Millimeters	
		Min.	Max.
A1	Component body width	4.70	5.10
A	Component body height	7.80	8.20
T	Component body thickness	3.70	4.10
d	Lead wire diameter	0.35	0.55
d1	Lead wire diameter 1	0.60	0.80
P	Pitch of component	12.40	13.00
P0	Feed hole pitch	12.50	12.90
P2	Hole center to component center	6.05	6.65
F1, F2	Lead to lead distance	2.20	2.80
Δh	Component alignment, F-R	-1.00	1.00
W	Tape width	17.50	19.00
W0	Hole down tape width	5.50	6.50
W1	Hole position	8.50	9.50
W2	Hole down tape position	-	1.00
H	Height of component from tape center	19.00	21.00
H0	Lead wire clinch height	15.50	16.50
L1	Lead wire (tape portion)	2.50	-
D0	Feed hole diameter	3.80	4.20
t1	Taped lead thickness	0.35	0.45
t2	Carrier tape thickness	0.15	0.25
P1	Position of hole	3.55	4.15
ΔP	Component alignment	-1.00	1.00

Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

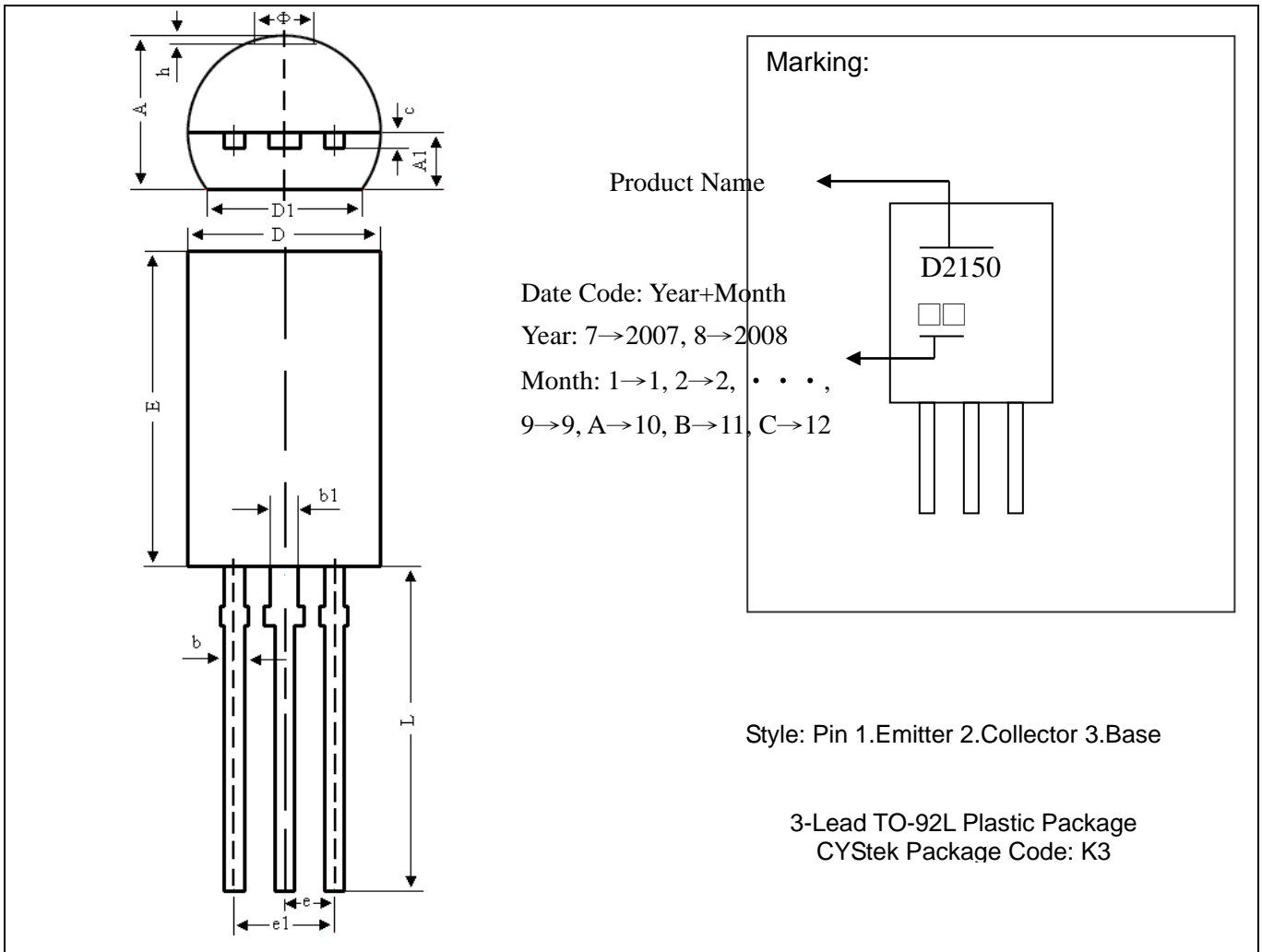
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (Tl)	183°C	217°C
- Time (tl)	60-150 seconds	60-150 seconds
Peak Temperature(Tp)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-92L Dimension



*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.146	0.161	3.700	4.100	E	0.307	0.323	7.800	8.200
A1	0.050	0.062	1.280	1.580	e	*0.05		*1.270	
b	0.014	0.022	0.350	0.550	e1	0.096	0.104	2.440	2.640
b1	0.024	0.031	0.600	0.800	L	0.543	0.559	13.800	14.200
c	0.014	0.018	0.350	0.450	φ	-	0.063	-	1.600
D	0.185	0.201	4.700	5.100	h	0.000	0.012	0.000	0.300
D1	0.157	-	4.000	-					

Notes: 1. Controlling dimension: millimeters.
 2. Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3. If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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