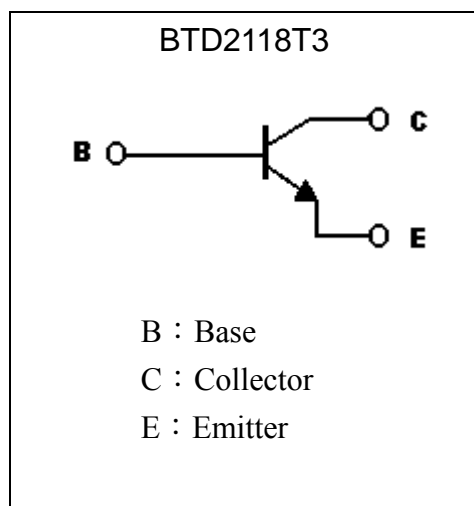
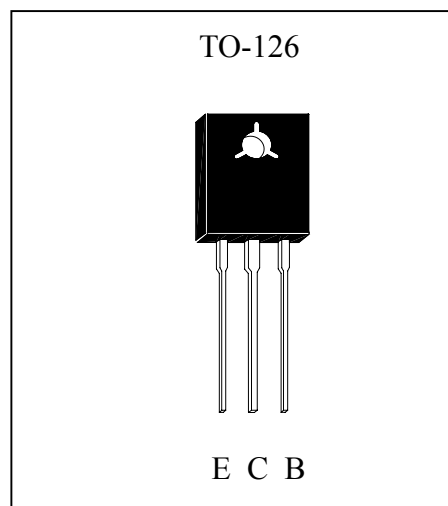


Silicon NPN Epitaxial Planar Transistor

BTD2118T3

Description

- High BV_{CEO}
- High current capability
- Pb-free package

Symbol

Outline

Absolute Maximum Ratings ($T_a=25^{\circ}\text{C}$)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V_{CBO}	80	V
Collector-Emitter Voltage	V_{CEO}	30	V
Emitter-Base Voltage	V_{EBO}	7	V
Collector Current (DC)	I_C	5	A
Collector Current (Pulse)	I_{CP}	8 (Note)	A
Power Dissipation @ $T_A=25^{\circ}\text{C}$	P_D	1	W
Power Dissipation @ $T_c=25^{\circ}\text{C}$	P_D	15	W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.33	$^{\circ}\text{C}/\text{W}$
Junction Temperature	T_j	150	$^{\circ}\text{C}$
Storage Temperature	T_{stg}	-55~+150	$^{\circ}\text{C}$

 Note : Single Pulse , $P_w \leq 380\mu\text{s}$, Duty $\leq 2\%$.

**Characteristics** (Ta=25°C)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV _{CBO}	80	-	-	V	I _C =50μA, I _E =0
BV _{CEO}	30	-	-	V	I _C =1mA, I _B =0
BV _{EBO}	7	-	-	V	I _E =50μA, I _C =0
I _{CBO}	-	-	1	μA	V _{CB} =80V, I _E =0
I _{EBO}	-	-	1	μA	V _{EB} =6V, I _C =0
*V _{CE(sat)}	-	-	0.5	V	I _C =3A, I _B =100mA
*V _{CE(sat)}	-	-	0.6	V	I _C =3A, I _B =60mA
*V _{BE(sat)}	-	-	1.2	V	I _C =3A, I _B =100mA
*h _{FE1}	260	-	-	-	V _{CE} =2V, I _C =20mA
*h _{FE2}	300	-	600	-	V _{CE} =2V, I _C =500mA
*h _{FE3}	200	-	-	-	V _{CE} =2V, I _C =2A
f _T	-	150	-	MHz	V _{CE} =6V, I _C =500mA
C _{ob}	-	-	50	pF	V _{CB} =10V, I _E =0, f=1MHz

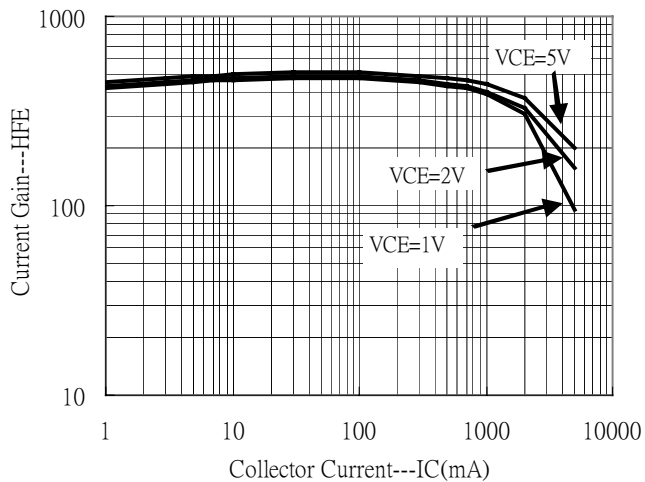
*Pulse Test: Pulse Width ≤380μs, Duty Cycle≤2%

Ordering Information

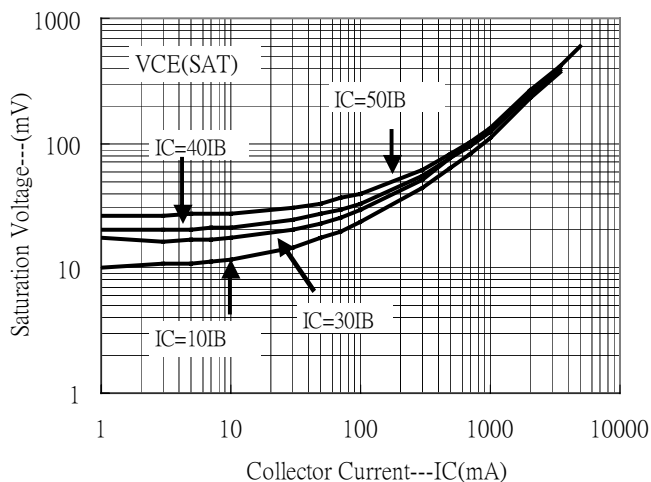
Device	Package	Shipping	Marking
BTD2118T3	TO-126 (Pb-free)	250 pcs / bag, 10 bags / box	D2118

Characteristic Curves

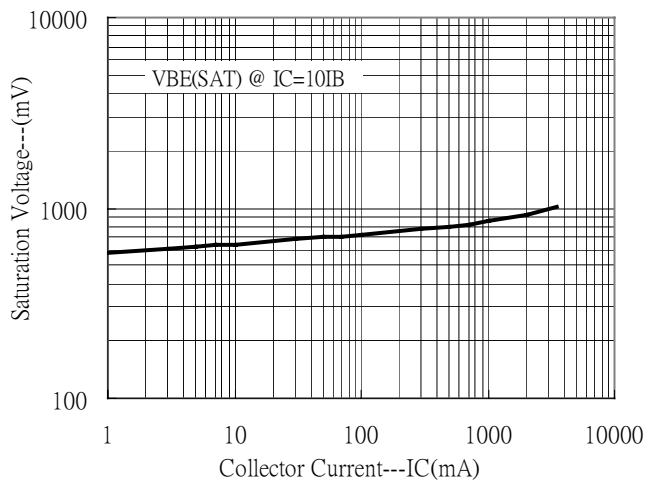
Current Gain vs Collector Current



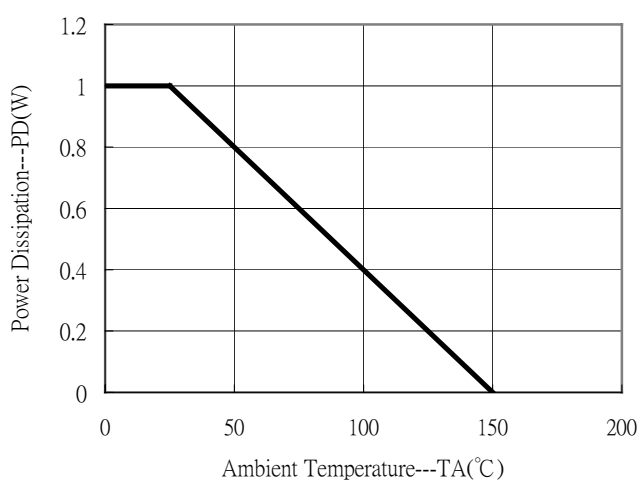
Saturation Voltage vs Collector Current



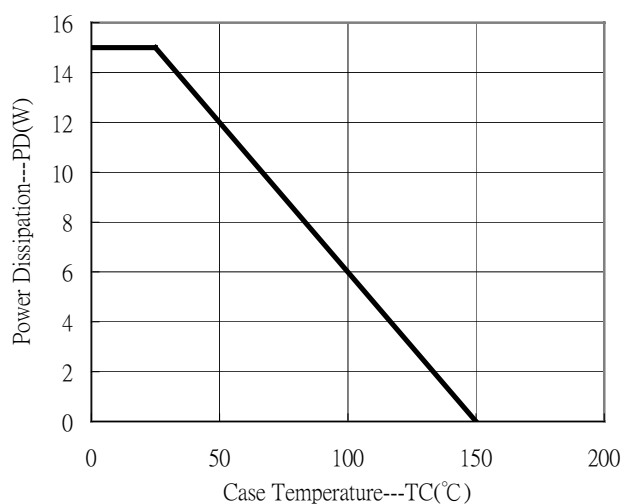
Saturation Voltage vs Collector Current



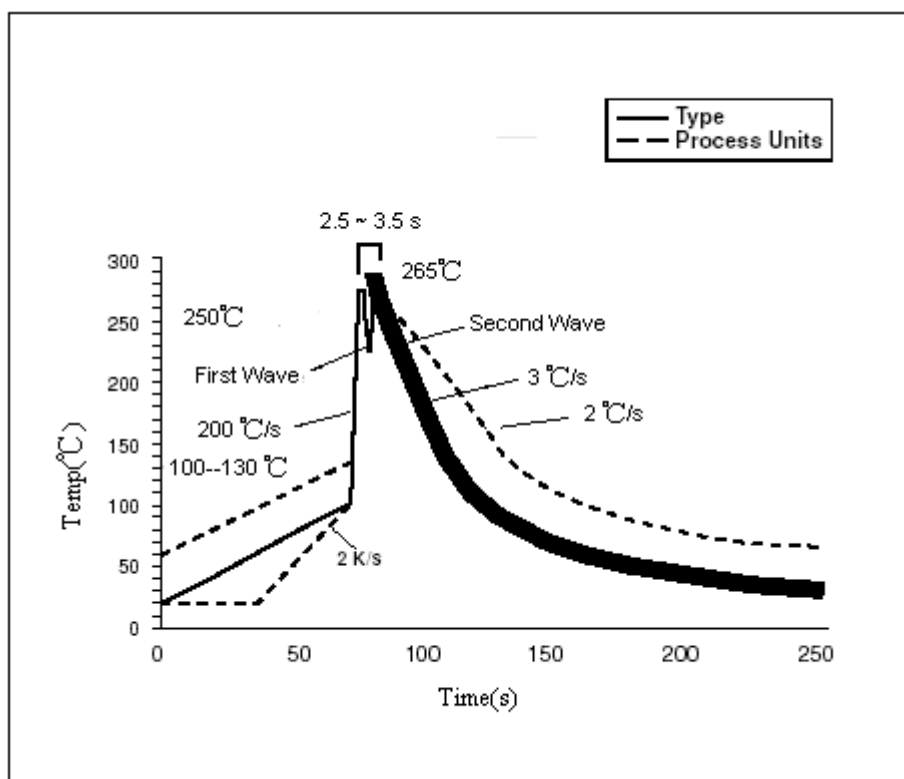
Power Derating Curve



Power Derating Curve



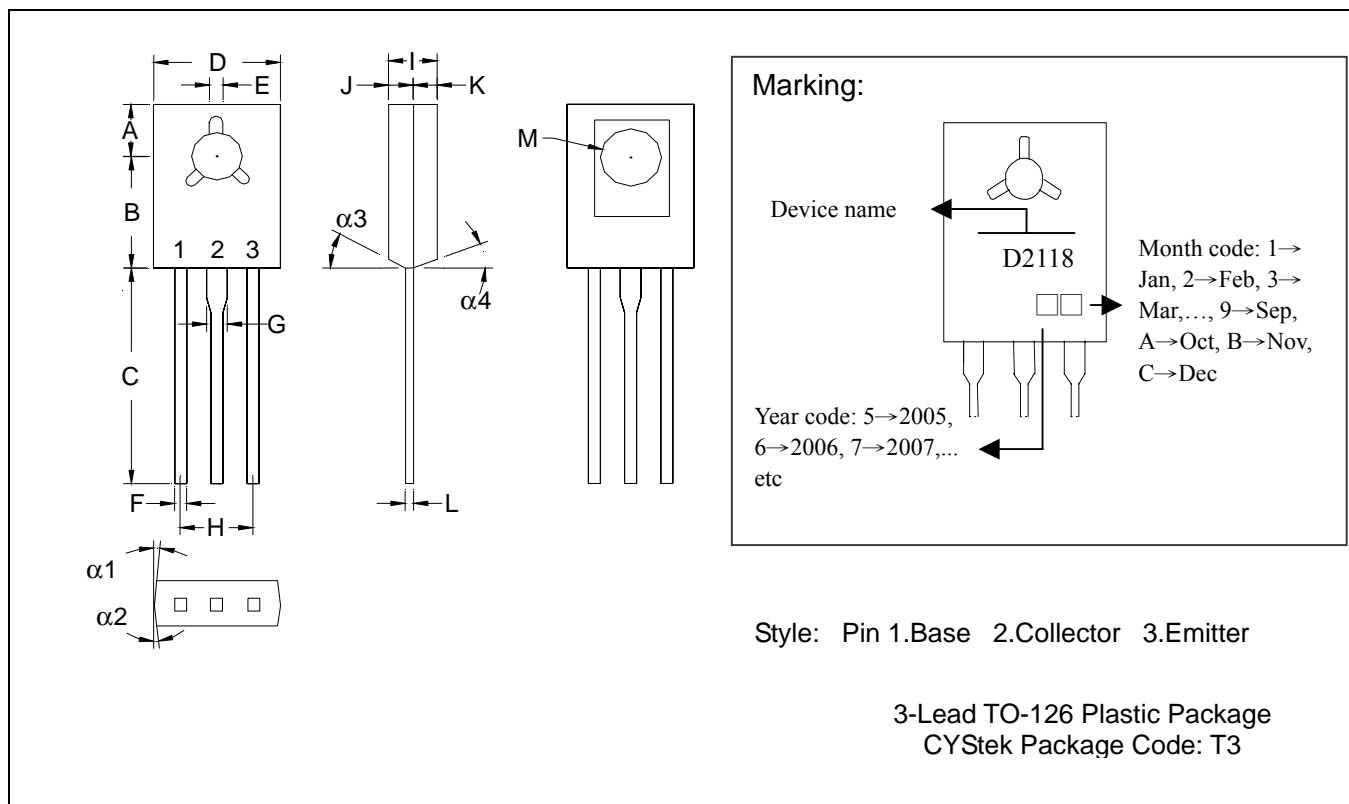
Recommended temperature profile for wave soldering



Recommendation:

1. Preheat temperature at solder side must be between 100 and 130 °C for 80 to 100 seconds.
2. Temperature ramp-up rate : 1~2 °C/s
3. The temperature gradient between preheat and wave soldering must be smaller than +100°C.
4. Terminations must go through the wave simultaneously.
5. Travel through the wave from 255 to 260°C for 2.5 to 3.5 seconds
6. Temperature ramp-down rate : 2~3 °C/s

TO-126 Dimension



*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
$\alpha 1$	-	*3°	-	*3°	F	0.0280	0.0319	0.71	0.81
$\alpha 2$	-	*3°	-	*3°	G	0.0480	0.0520	1.22	1.32
$\alpha 3$	-	*3°	-	*3°	H	0.1709	0.1890	4.34	4.80
$\alpha 4$	-	*3°	-	*3°	I	0.0950	0.1050	2.41	2.66
A	0.1500	0.1539	3.81	3.91	J	0.0450	0.0550	1.14	1.39
B	0.2752	0.2791	6.99	7.09	K	0.0450	0.0550	1.14	1.39
C	0.5315	0.6102	13.50	15.50	L	-	*0.0217	-	*0.55
D	0.2854	0.3039	7.52	7.72	M	0.1378	0.1520	3.50	3.86
E	0.0374	0.0413	0.95	1.05					

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: 42 Alloy; solder plating
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0

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