

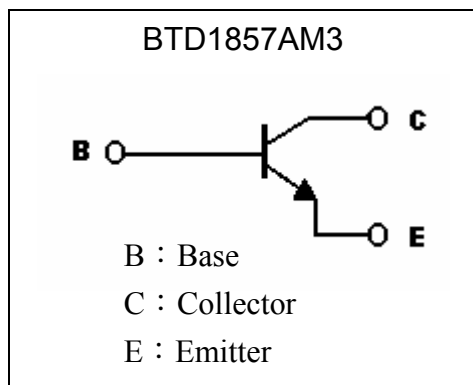
**Silicon NPN Epitaxial Planar Transistor**  
**BTD1857AM3**

$BV_{CEO}$	160V
$I_C$	1.5A
$R_{CESAT(MAX)}$	0.3 $\Omega$

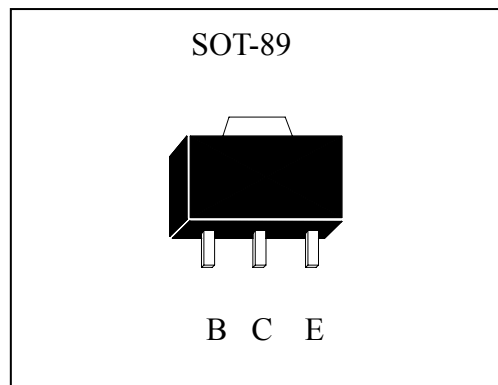
**Description**

- High  $BV_{CEO}$
- High current capability
- Complementary to BTB1236AM3
- Pb-free lead plating and halogen-free package

**Symbol**

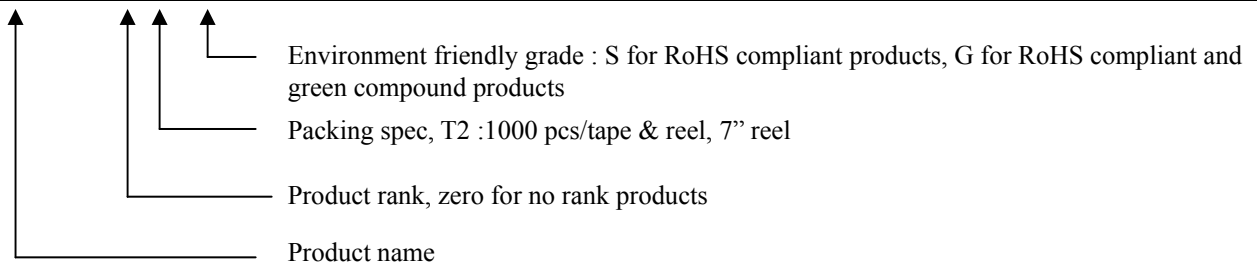


**Outline**



**Ordering Information**

Device	Package	Shipping
BTD1857AM3-X-T2-G	SOT-89 (Pb-free lead plating and halogen-free package)	1000 pcs / Tape & Reel



**Absolute Maximum Ratings (Ta=25°C)**

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V <sub>CB0</sub>	180	V
Collector-Emitter Voltage	V <sub>CEO</sub>	160	V
Emitter-Base Voltage	V <sub>EBO</sub>	5	V
Collector Current (DC)	I <sub>C</sub>	1.5	A
Collector Current (Pulse)	I <sub>CP</sub>	3	A
Power Dissipation	P <sub>D</sub>	0.6	W
		1 (Note 1)	
		2 (Note 2)	
Operating Junction and Storage Temperature Range	T <sub>j</sub> ; T <sub>stg</sub>	-55~+150	°C

Note : 1. When mounted on FR-4 PCB with area measuring 10×10×1 mm  
2 . When mounted on ceramic with area measuring 40×40×1 mm

**Thermal Characteristics**

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction to Ambient	R <sub>θJA</sub>	208	°C/W
		125 (Note 1)	
		62.5 (Note 2)	
Thermal Resistance, Junction to Case	R <sub>θJC</sub>	39.3	°C/W

Note : 1. When mounted on FR-4 PCB with area measuring 10×10×1 mm  
2 . When mounted on ceramic with area measuring 40×40×1 mm

**Characteristics (Ta=25°C)**

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV <sub>CB0</sub>	180	-	-	V	I <sub>C</sub> =50μA, I <sub>E</sub> =0
BV <sub>CEO</sub>	160	-	-	V	I <sub>C</sub> =1mA, I <sub>B</sub> =0
BV <sub>EBO</sub>	5	-	-	V	I <sub>E</sub> =50μA, I <sub>C</sub> =0
I <sub>CB0</sub>	-	-	1	μA	V <sub>CB</sub> =160V, I <sub>E</sub> =0
I <sub>EBO</sub>	-	-	1	μA	V <sub>EB</sub> =4V, I <sub>C</sub> =0
*V <sub>CE(sat)</sub>	-	-	0.3	V	I <sub>C</sub> =1A, I <sub>B</sub> =100mA
*R <sub>CE(sat)</sub>	-	-	0.3	Ω	I <sub>C</sub> =1A, I <sub>B</sub> =100mA
*V <sub>BE(on)</sub>	-	-	1.5	V	V <sub>CE</sub> =5V, I <sub>C</sub> =150mA
h <sub>FE1</sub>	180	-	390	-	V <sub>CE</sub> =5V, I <sub>C</sub> =150mA
h <sub>FE2</sub>	30	-	-	-	V <sub>CE</sub> =5V, I <sub>C</sub> =500mA
f <sub>T</sub>	-	140	-	MHz	V <sub>CE</sub> =5V, I <sub>C</sub> =150mA
C <sub>ob</sub>	-	27	-	pF	V <sub>CB</sub> =10V, I <sub>E</sub> =0, f=1MHz

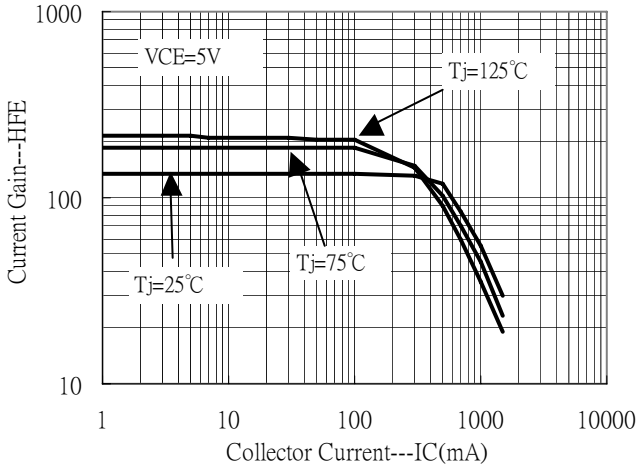
\*Pulse Test: Pulse Width ≤380μs, Duty Cycle≤2%

**Classification Of h<sub>FE</sub> 1**

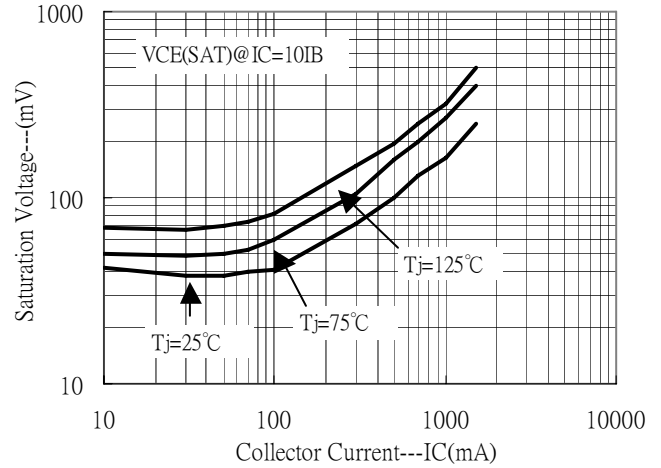
Rank	R
Range	180~390

**Characteristic Curves**

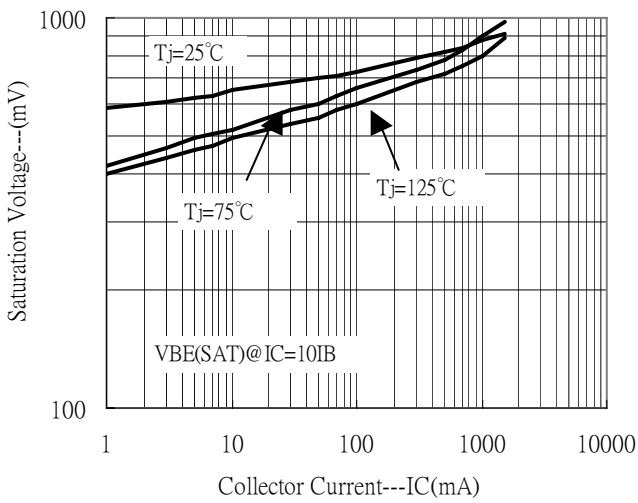
Current Gain vs Collector Current



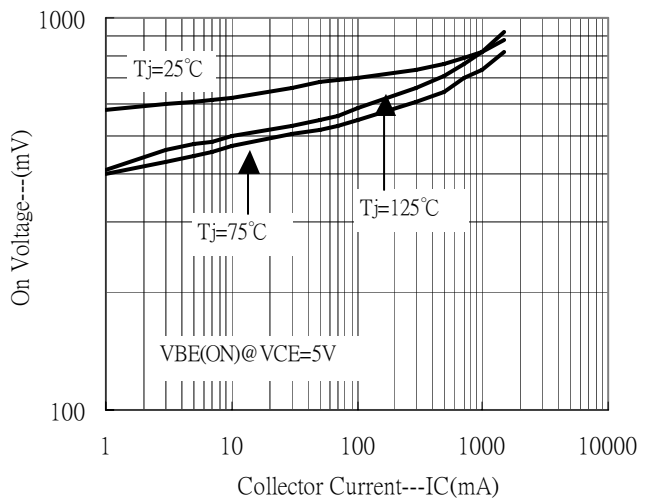
Saturation Voltage vs Collector Current



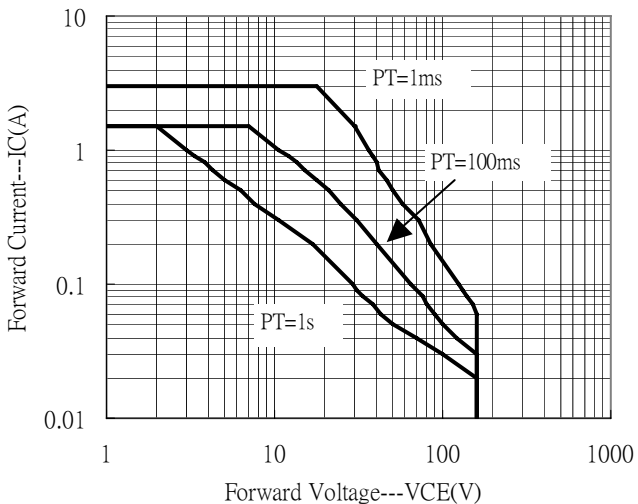
Saturation Voltage vs Collector Current



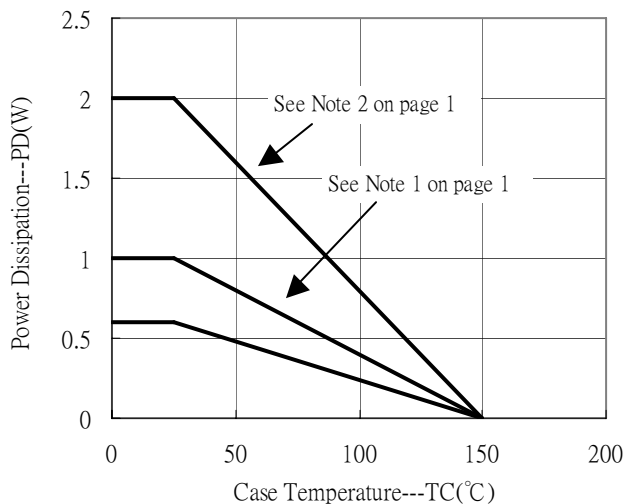
On Voltage vs Collector Current



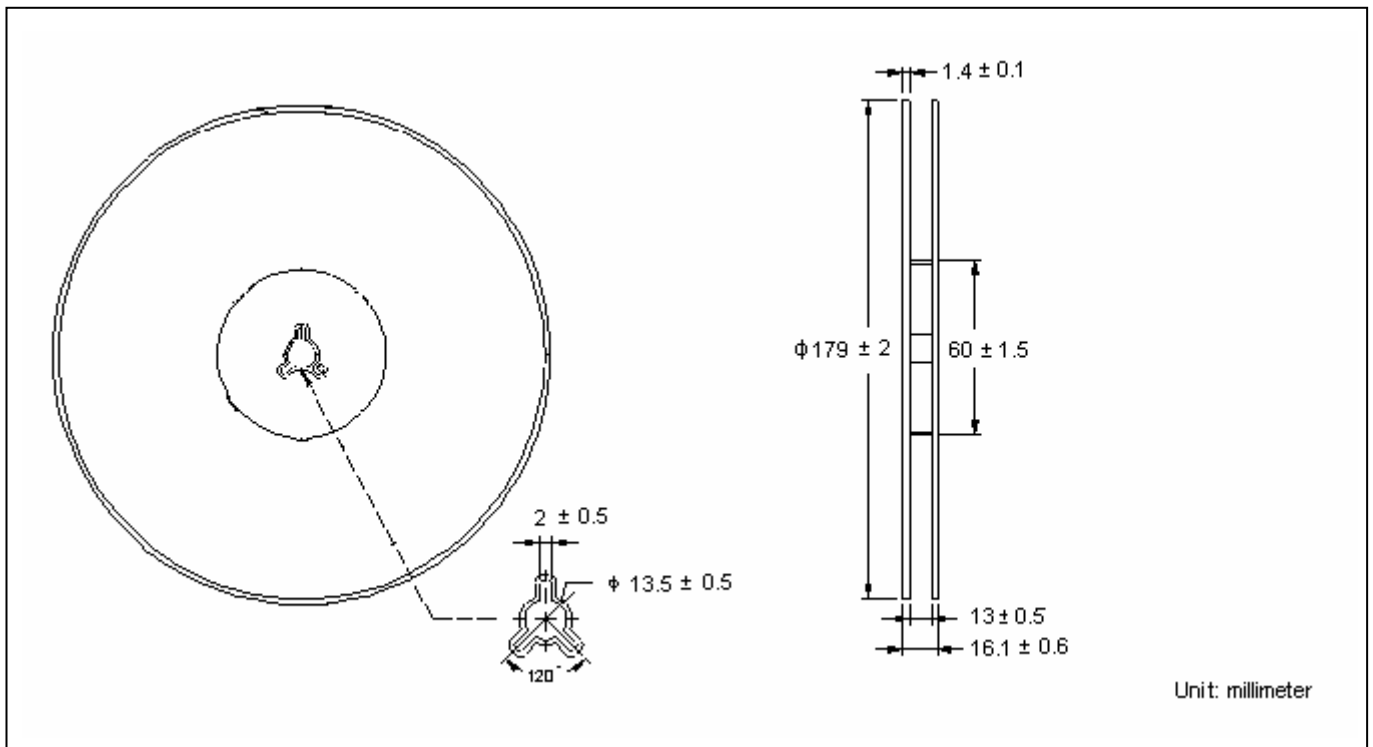
Safe Operating Area



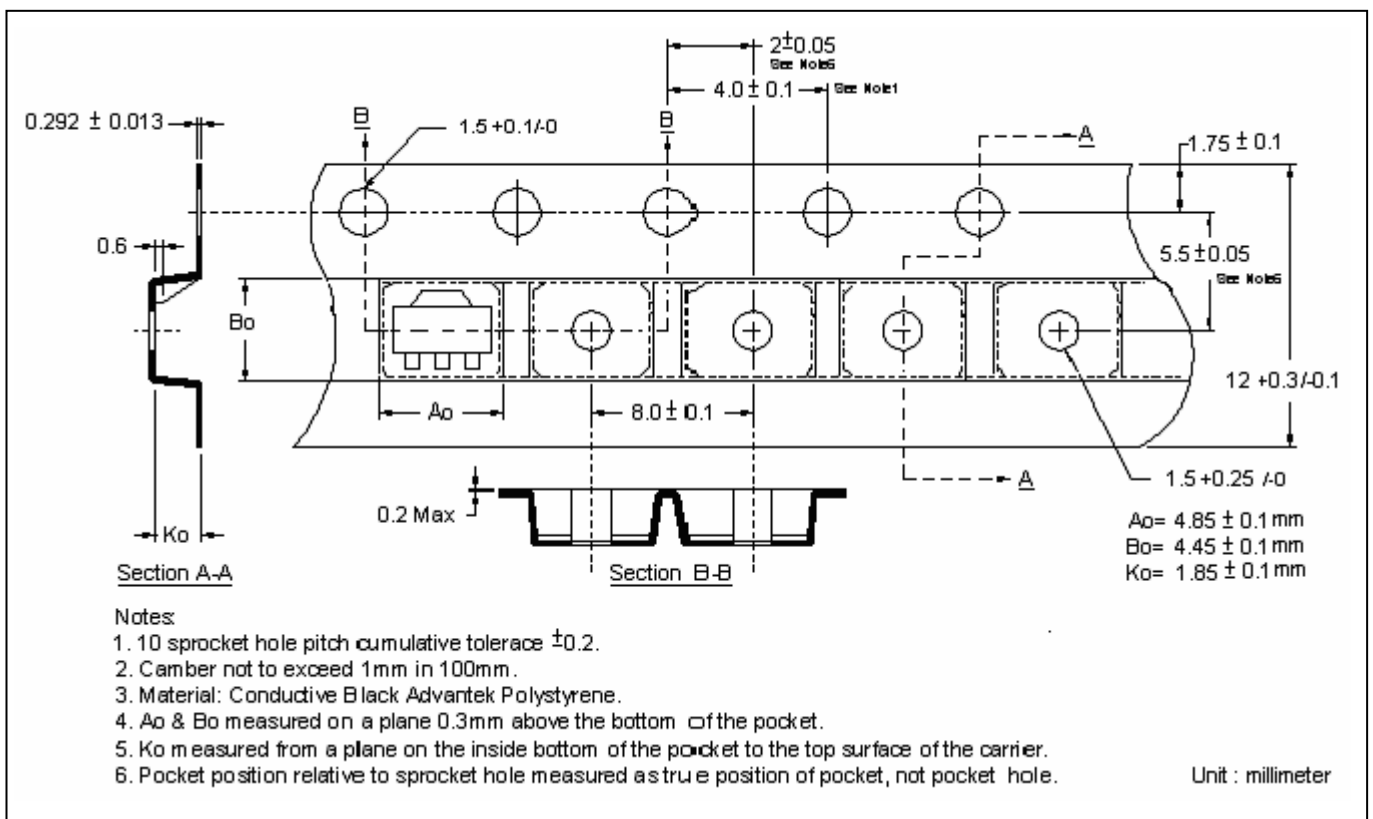
Power Derating Curve



**Reel Dimension**



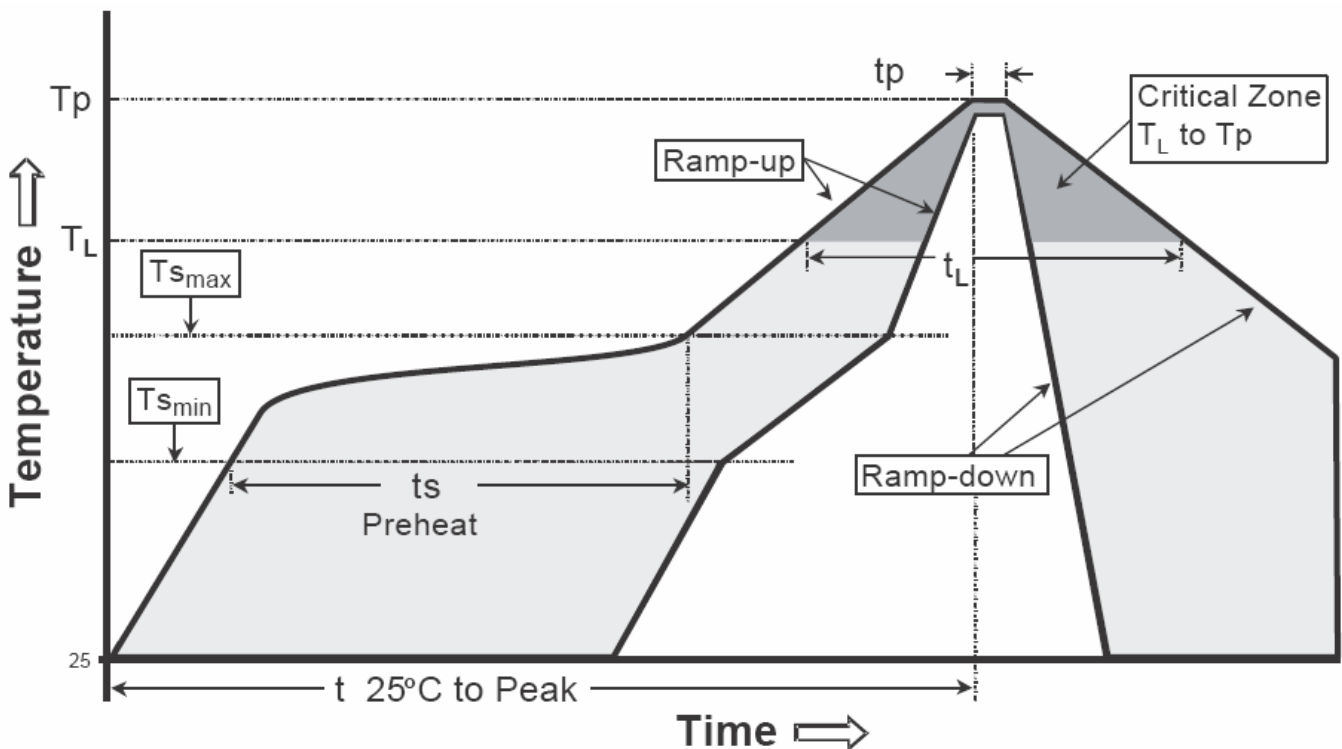
**Carrier Tape Dimension**



**Recommended wave soldering condition**

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

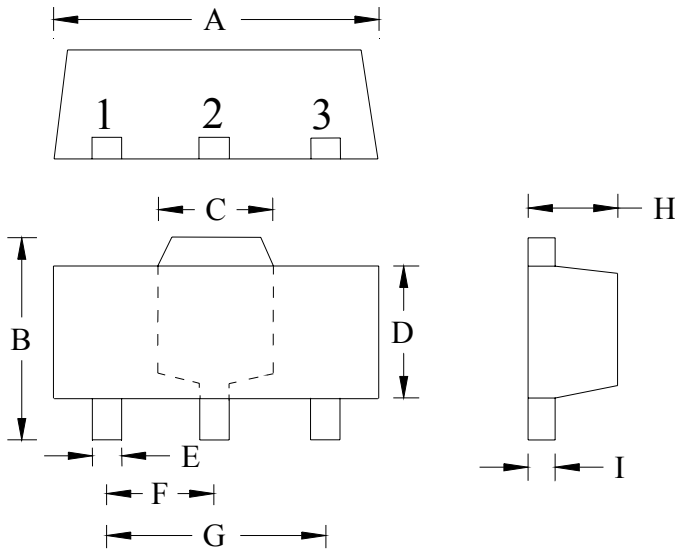
**Recommended temperature profile for IR reflow**



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (Tl)	183°C	217°C
- Time (tl)	60-150 seconds	60-150 seconds
Peak Temperature(Tp)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

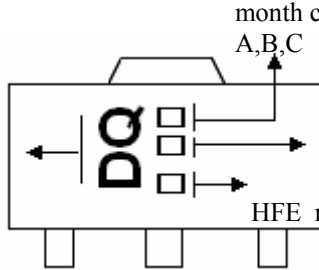
Note : All temperatures refer to topside of the package, measured on the package body surface.

**SOT-89 Dimension**



The diagram shows three views of the SOT-89 package: a top view with dimensions A, B, C, D, E, F, G, and three pins labeled 1, 2, and 3; a side view with dimensions H and I; and a perspective view. The top view shows a trapezoidal shape with three pins extending downwards. The side view shows the thickness of the package. The perspective view shows the package from an angle, highlighting the trapezoidal shape and the pins.

**Marking:**



The marking diagram shows the layout of markings on the package. It includes a 'Product Code' (DQ), a 'month code' (1-9, A, B, C), a 'Year code' (6 for 2006, 7 for 2007, etc.), and an 'HFE rank'.

Style: Pin 1. Base 2. Collector 3. Emitter

3-Lead SOT-89 Plastic  
 Surface Mounted Package  
 CYStek Package Code: M3

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1732	0.1811	4.40	4.60	F	0.0591	TYP	1.50	TYP
B	0.1551	0.1673	3.94	4.25	G	0.1181	TYP	3.00	TYP
C	0.0610	REF	1.55	REF	H	0.0551	0.0630	1.40	1.60
D	0.0906	0.1024	2.30	2.60	I	0.0138	0.0173	0.35	0.44
E	0.0126	0.0205	0.32	0.52					

**Notes:** 1. Controlling dimension: millimeters.  
 2. Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.  
 3. If there is any question with packing specification or packing method, please contact your local CYStek sales office.

**Material:**

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0

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