

# Silicon NPN Epitaxial Planar Transistor

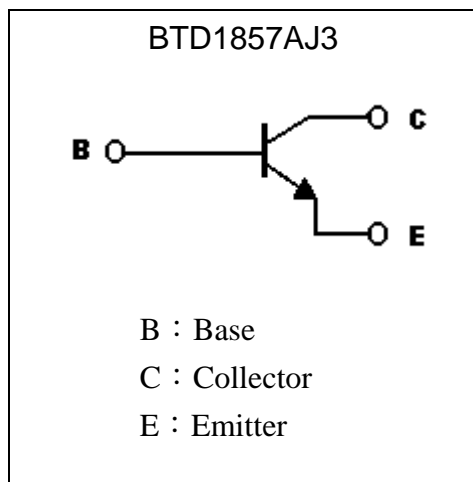
## BTD1857AJ3

$BV_{CEO}$	160V
$I_C$	1.5A

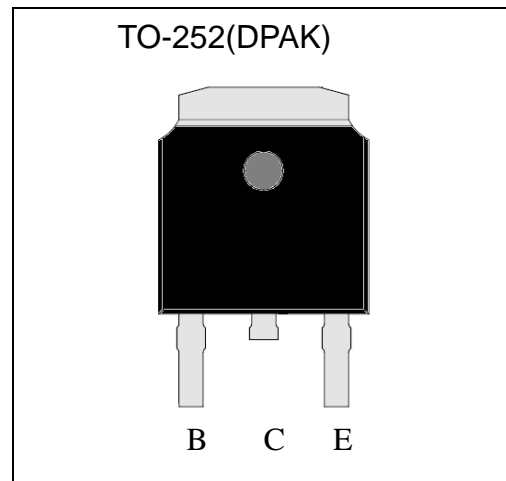
### Description

- High  $BV_{CEO}$
- High current capability
- Complementary to BTB1236AJ3
- Pb-free lead plating and halogen-free package

### Symbol

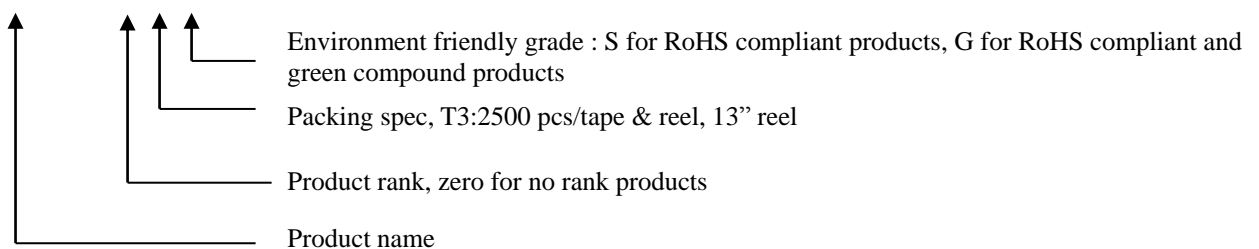


### Outline



### Ordering Information

Device	Package	Shipping
BTD1857AJ3-X-T3-G	TO-252 (Pb-free lead plating and halogen-free package)	2500 pcs / Tape & Reel



**Absolute Maximum Ratings** (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V <sub>CB0</sub>	180	V
Collector-Emitter Voltage	V <sub>CEO</sub>	160	V
Emitter-Base Voltage	V <sub>EBO</sub>	5	V
Collector Current (DC)	I <sub>C</sub>	1.5	A
Collector Current (Pulse)	I <sub>CP</sub>	3	A
Power Dissipation @T <sub>A</sub> =25°C	P <sub>D</sub>	1	W
Power Dissipation @T <sub>C</sub> =25°C		10	W
Junction Temperature	T <sub>j</sub>	150	°C
Storage Temperature	T <sub>stg</sub>	-55~+150	°C

**Thermal Data**

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	R <sub>th,j-c</sub>	12.5	°C/W
Thermal Resistance, Junction-to-ambient, max	R <sub>th,j-a</sub>	125	°C/W

**Characteristics** (Ta=25°C)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV <sub>CB0</sub>	180	-	-	V	I <sub>C</sub> =50μA, I <sub>E</sub> =0
BV <sub>CEO</sub>	160	-	-	V	I <sub>C</sub> =1mA, I <sub>B</sub> =0
BV <sub>EBO</sub>	5	-	-	V	I <sub>E</sub> =50μA, I <sub>C</sub> =0
I <sub>CB0</sub>	-	-	1	μA	V <sub>CB</sub> =160V, I <sub>E</sub> =0
I <sub>EBO</sub>	-	-	1	μA	V <sub>EB</sub> =4V, I <sub>C</sub> =0
*V <sub>CE(sat)</sub>	-	-	0.6	V	I <sub>C</sub> =1A, I <sub>B</sub> =100mA
*V <sub>BE(on)</sub>	-	-	1.5	V	V <sub>CE</sub> =5V, I <sub>C</sub> =150mA
h <sub>FE1</sub>	180	-	390	-	V <sub>CE</sub> =5V, I <sub>C</sub> =150mA
h <sub>FE2</sub>	30	-	-	-	V <sub>CE</sub> =5V, I <sub>C</sub> =500mA
f <sub>T</sub>	-	140	-	MHz	V <sub>CE</sub> =5V, I <sub>C</sub> =150mA
C <sub>ob</sub>	-	27	-	pF	V <sub>CB</sub> =10V, I <sub>E</sub> =0, f=1MHz

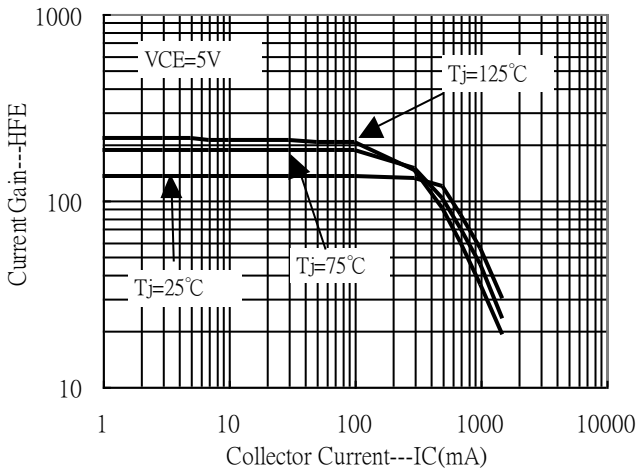
\*Pulse Test: Pulse Width ≤380μs, Duty Cycle≤2%

**Classification Of h<sub>FE</sub> 1**

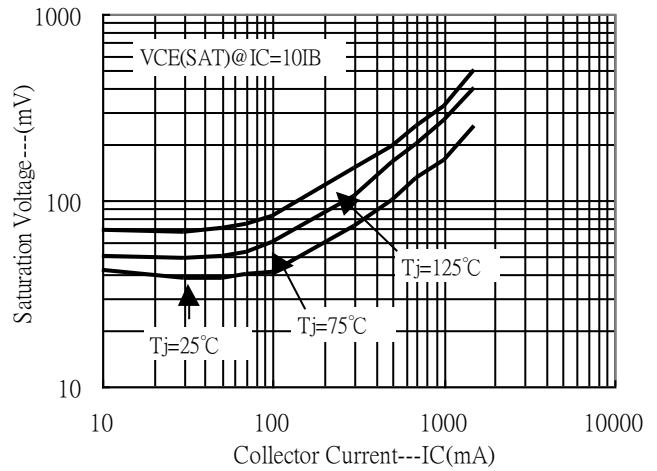
Rank	R
Range	180~390

**Typical Characteristics**

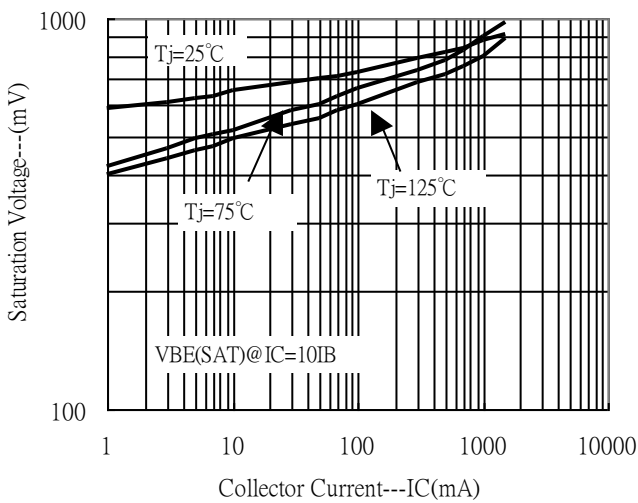
Current Gain vs Collector Current



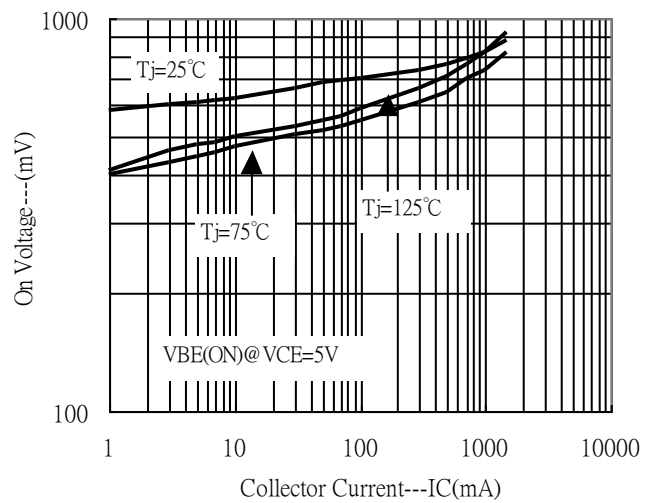
Saturation Voltage vs Collector Current



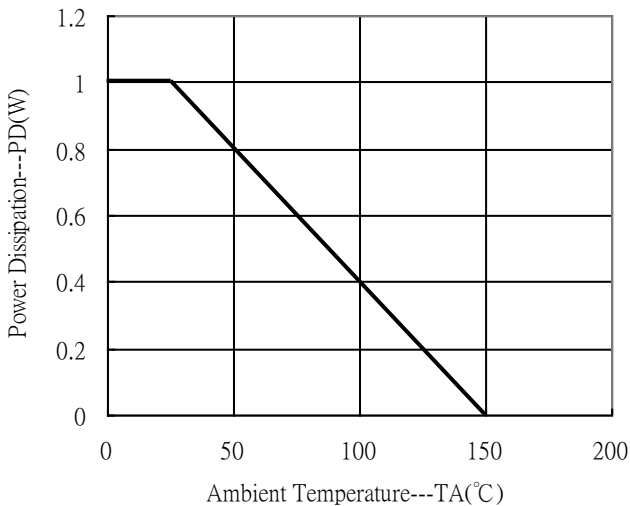
Saturation Voltage vs Collector Current



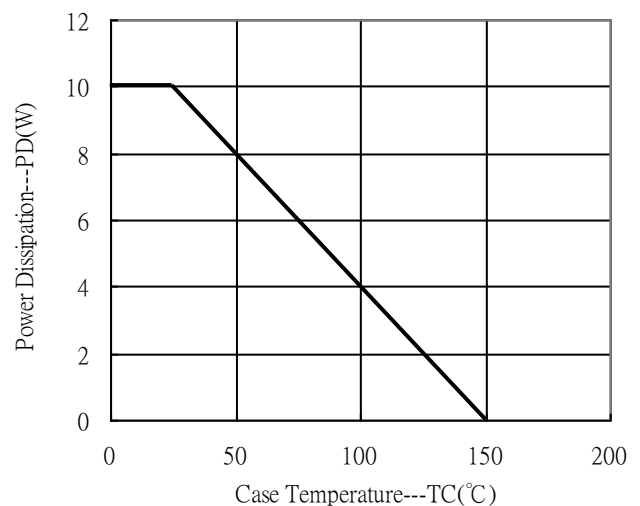
On Voltage vs Collector Current



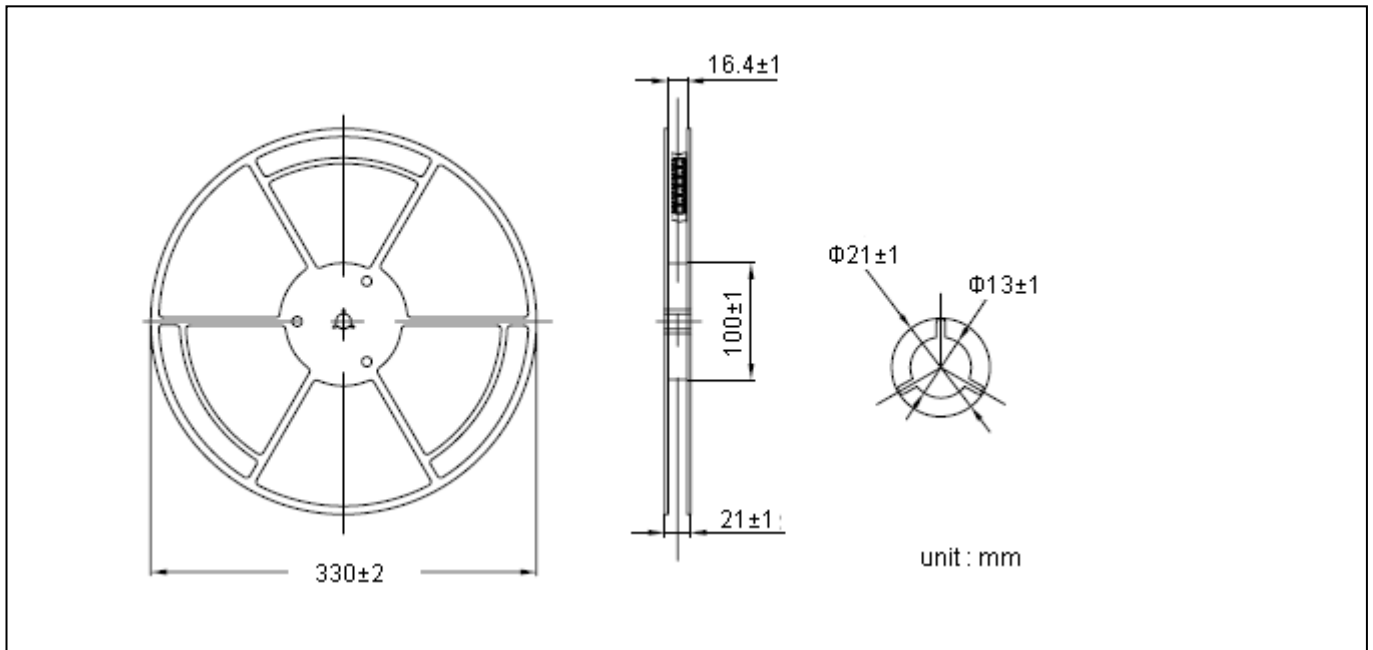
Power Derating Curve



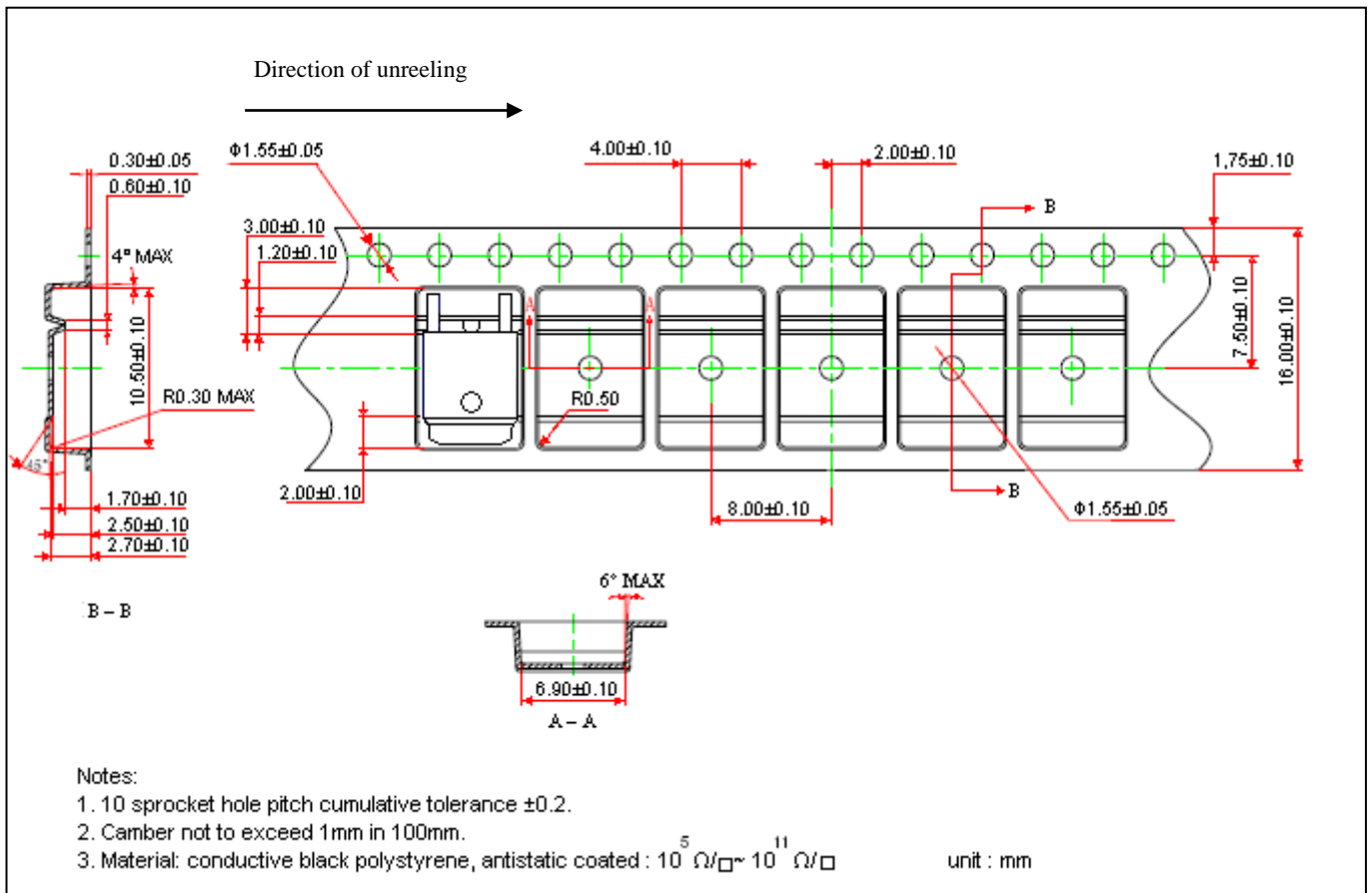
Power Derating Curve



**Reel Dimension**



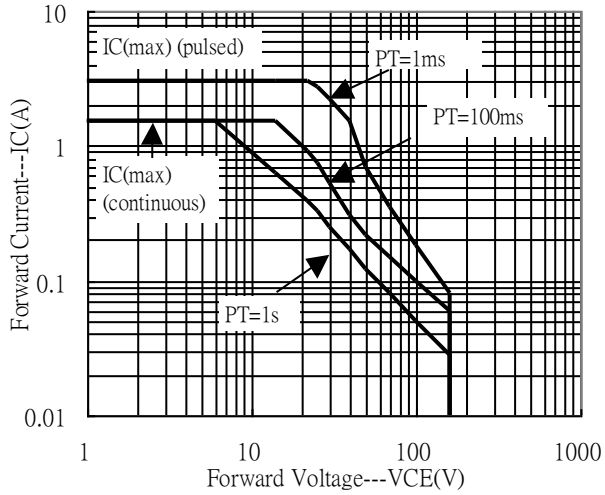
**Carrier Tape Dimension**





### Typical Characteristics(Cont.)

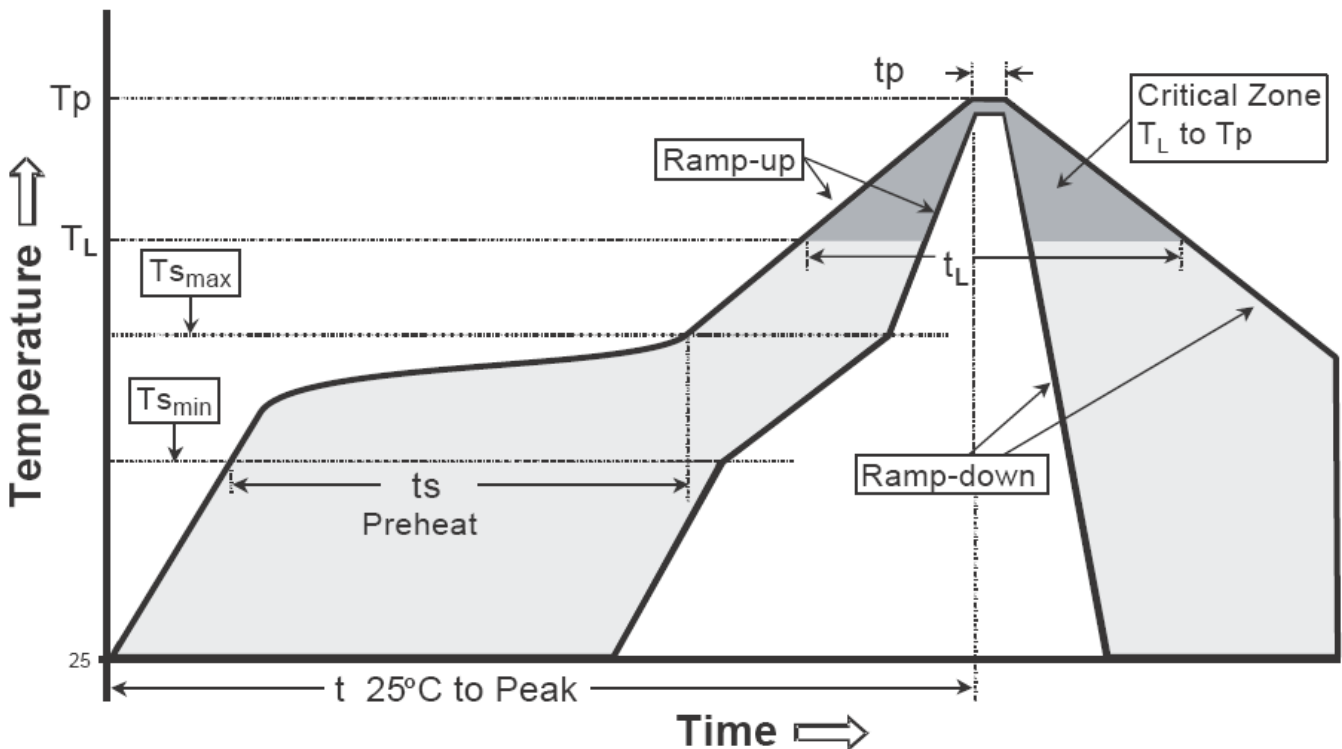
Safe Operating Area



**Recommended wave soldering condition**

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

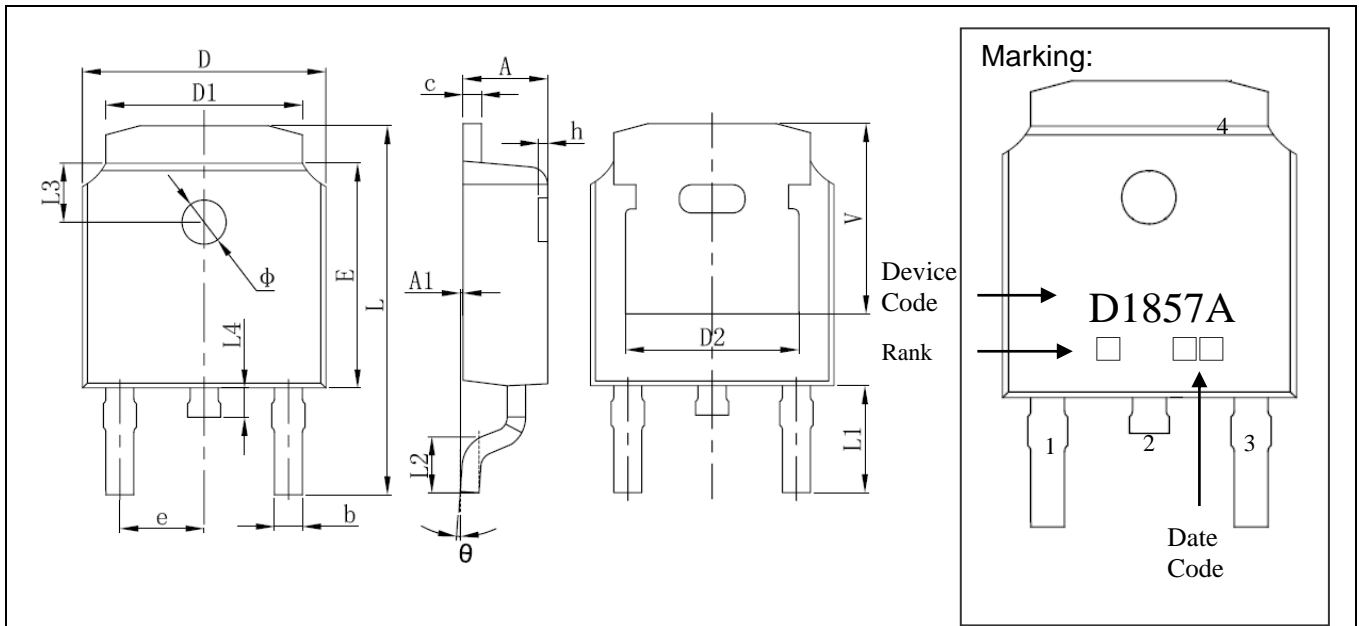
**Recommended temperature profile for IR reflow**



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T <sub>smax</sub> to T <sub>p</sub> )	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T <sub>s min</sub> )	100°C	150°C
-Temperature Max(T <sub>s max</sub> )	150°C	200°C
-Time(t <sub>s min</sub> to t <sub>s max</sub> )	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T <sub>L</sub> )	183°C	217°C
- Time (t <sub>L</sub> )	60-150 seconds	60-150 seconds
Peak Temperature(T <sub>p</sub> )	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

**TO-252 Dimension**



**3-Lead TO-252 Plastic Surface Mount Package**  
 CYStek Package Code: J3

Date Code :  
 First code : Year code, Last digit of Christian Year  
 Second Code : Month code, 1~9, A, B, C

Style: Pin 1.Base 2.Collector 3.Emitter 4.Collector

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.087	0.094	2.200	2.400	L	0.382	0.406	9.712	10.312
A1	0.000	0.005	0.000	0.127	L1	0.114	REF	2.900	REF
b	0.025	0.030	0.635	0.770	L2	0.055	0.067	1.400	1.700
c	0.018	0.023	0.460	0.580	L3	0.063	REF	1.600	REF
D	0.256	0.264	6.500	6.700	L4	0.024	0.039	0.600	1.000
D1	0.201	0.215	5.100	5.460	Φ	0.043	0.051	1.100	1.300
D2	0.190	REF	4.830	REF	θ	0°	8°	0°	8°
E	0.236	0.244	6.000	6.200	h	0.000	0.012	0.000	0.300
e	0.086	0.094	2.186	2.386	v	0.207	REF	5.250	REF

- Notes: 1.Controlling dimension: millimeters.  
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.  
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

**Material:**

- Lead : Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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