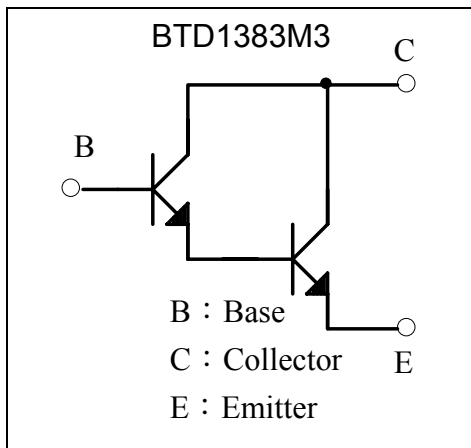
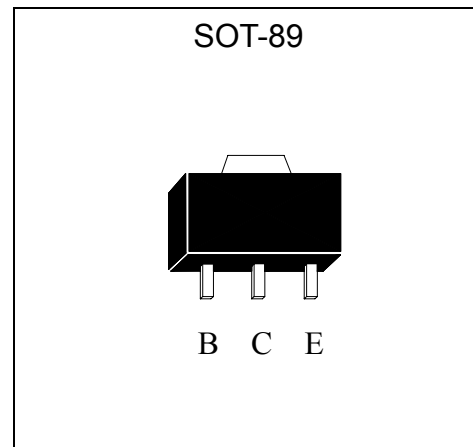


General Purpose NPN Epitaxial Planar Transistor

BTD1383M3

Description

- The BTD1383M3 is a darlington amplifier transistor.
- Pb-free package

Symbol

Outline

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V _{CB0}	40	V
Collector-Emitter Voltage	V _{CES}	32	V
Emitter-Base Voltage	V _{EBO}	10	V
Collector Current (DC)	I _C	0.3	A
Collector Current (Pulse)	I _{CP}	1.5 (Note 1)	A
Power Dissipation	P _d	0.6	W
		1 (Note 2)	W
		2 (Note 3)	W
Thermal Resistance, Junction to Ambient	R _{θJA}	208	°C/W
		125 (Note 2)	°C/W
		62.5 (Note 3)	°C/W
Junction Temperature	T _j	150	°C
Storage Temperature	T _{stg}	-55~+150	°C

Note : 1. Single Pulse Pw ≤ 350μs, Duty ≤ 2%.

2. When mounted on a FR-4 PCB with area measuring 10×10×1 mm.

3. When mounted on a ceramic board with area measuring 40×40×1mm.

**Characteristics (Ta=25°C)**

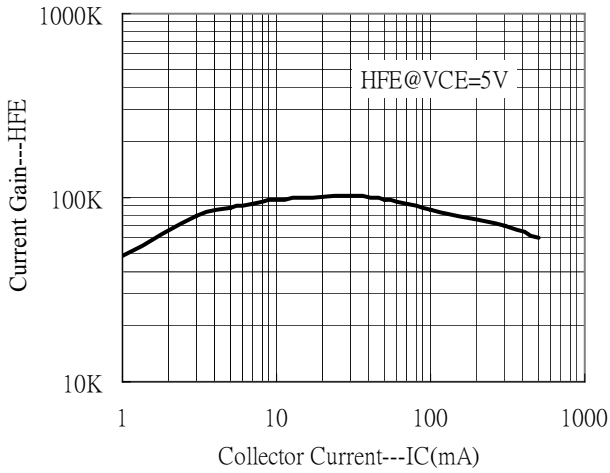
Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV_{CBO}	40	-	-	V	$I_C=100\mu A$
BV_{CES}	32	-	-	V	$I_C=1mA, R_{BE}=0\Omega$
BV_{EBO}	10	-	-	V	$I_E=100\mu A$
I_{CBO}	-	-	100	nA	$V_{CB}=30V$
I_{EBO}	-	-	100	nA	$V_{EB}=10V$
* $V_{CE(sat)}$	-	-	1.5	V	$I_C=200mA, I_B=0.4mA$
* h_{FE1}	10K	-	-		$V_{CE}=5V, I_C=10mA$
* h_{FE2}	20K	-	-		$V_{CE}=5V, I_C=100mA$
f_T	-	250	-	MHz	$V_{CE}=5V, I_C=10mA, f=100MHz$
Cob	-	5	-	pF	$V_{CB}=10V, I_E=0A, f=1MHz$

*Pulse Test: Pulse Width $\leq 380\mu s$, Duty Cycle $\leq 2\%$ **Ordering Information**

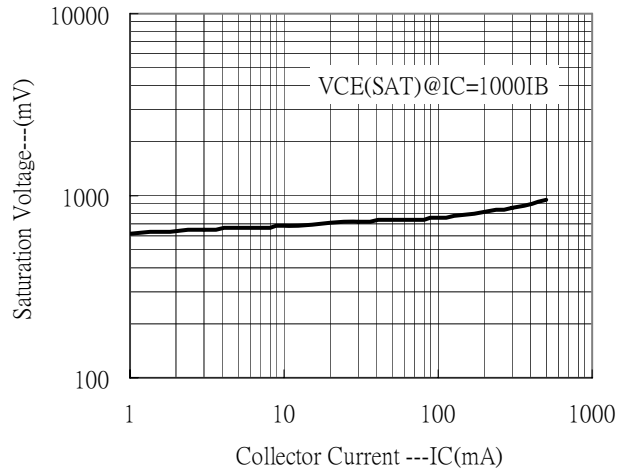
Device	Package	Shipping	Marking
BTD1383M3	SOT-89 (Pb-free)	1000 pcs / Tape & Reel	WA

Characteristic Curves

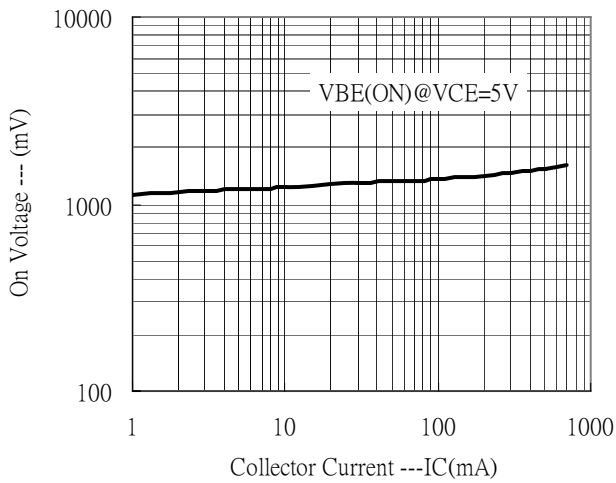
Current Gain vs Collector Current



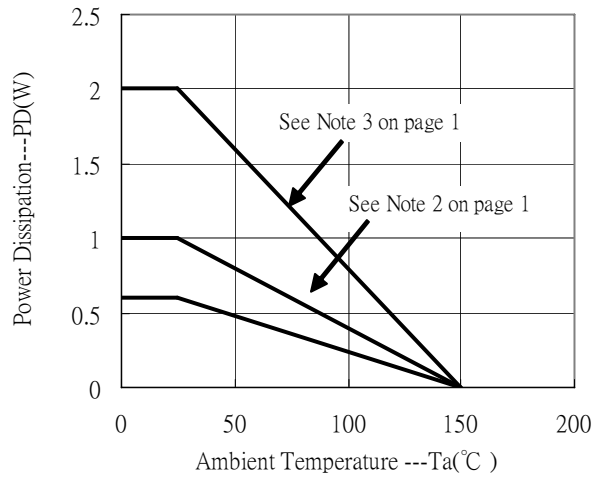
Saturation Voltage vs Collector Current



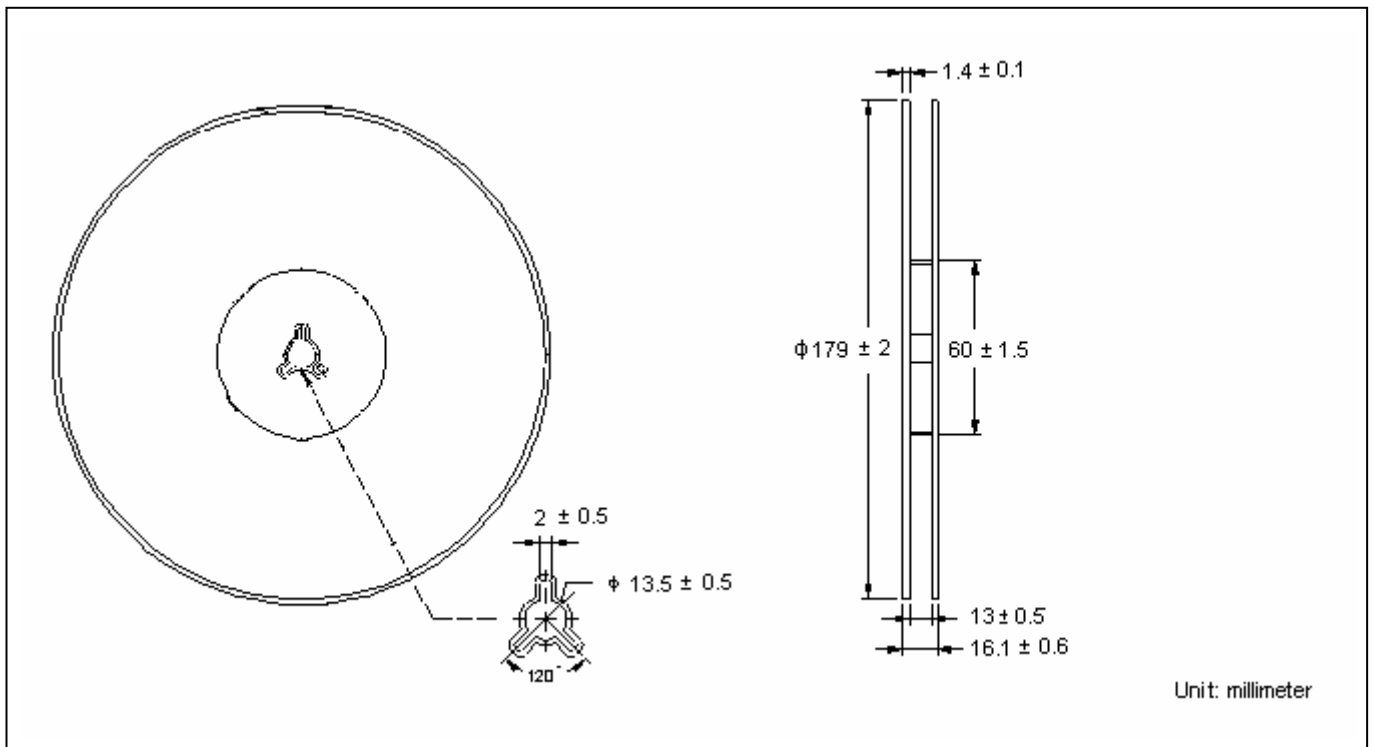
On Voltage vs Collector Current



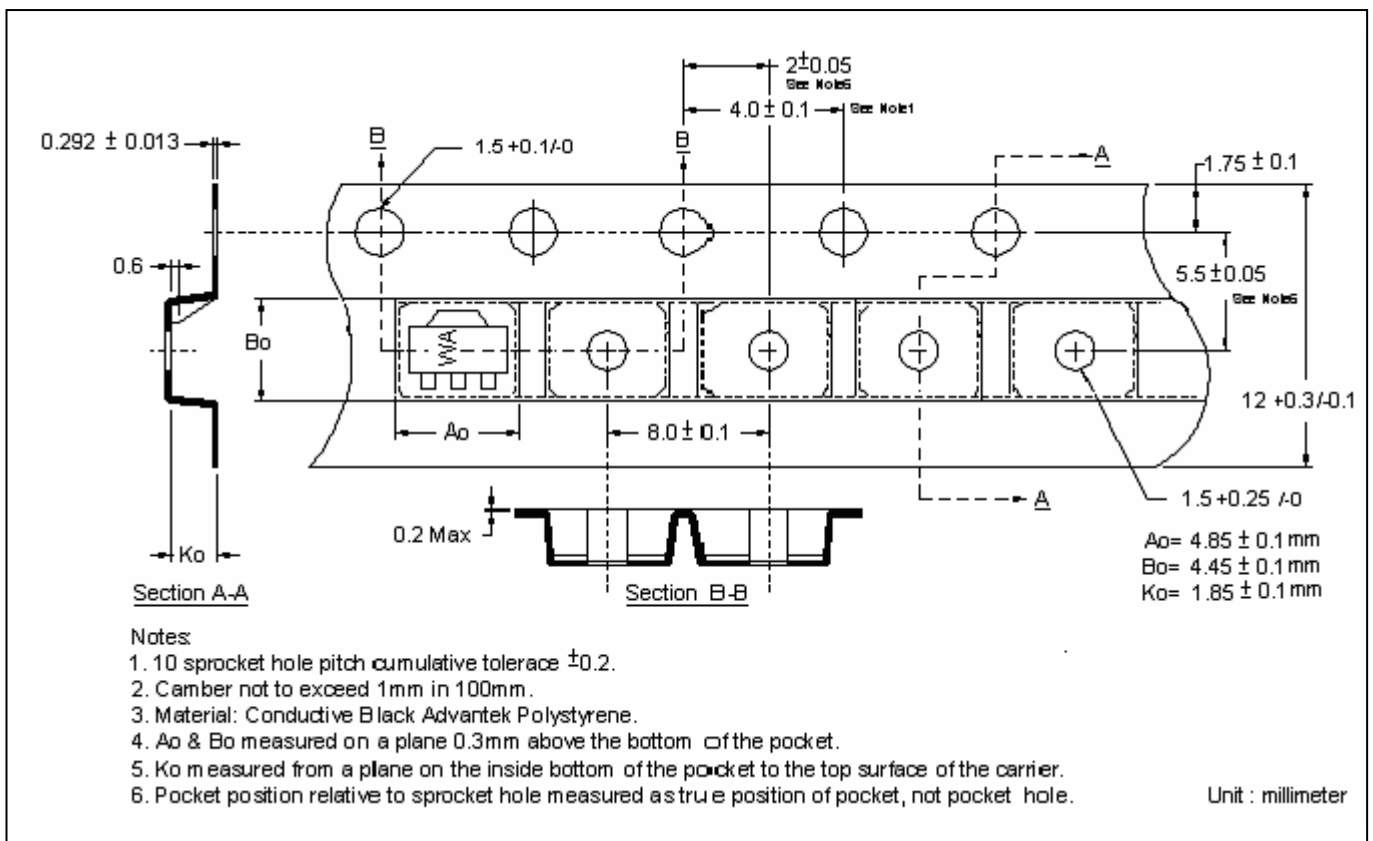
Power Derating Curves



Reel Dimension



Carrier Tape Dimension



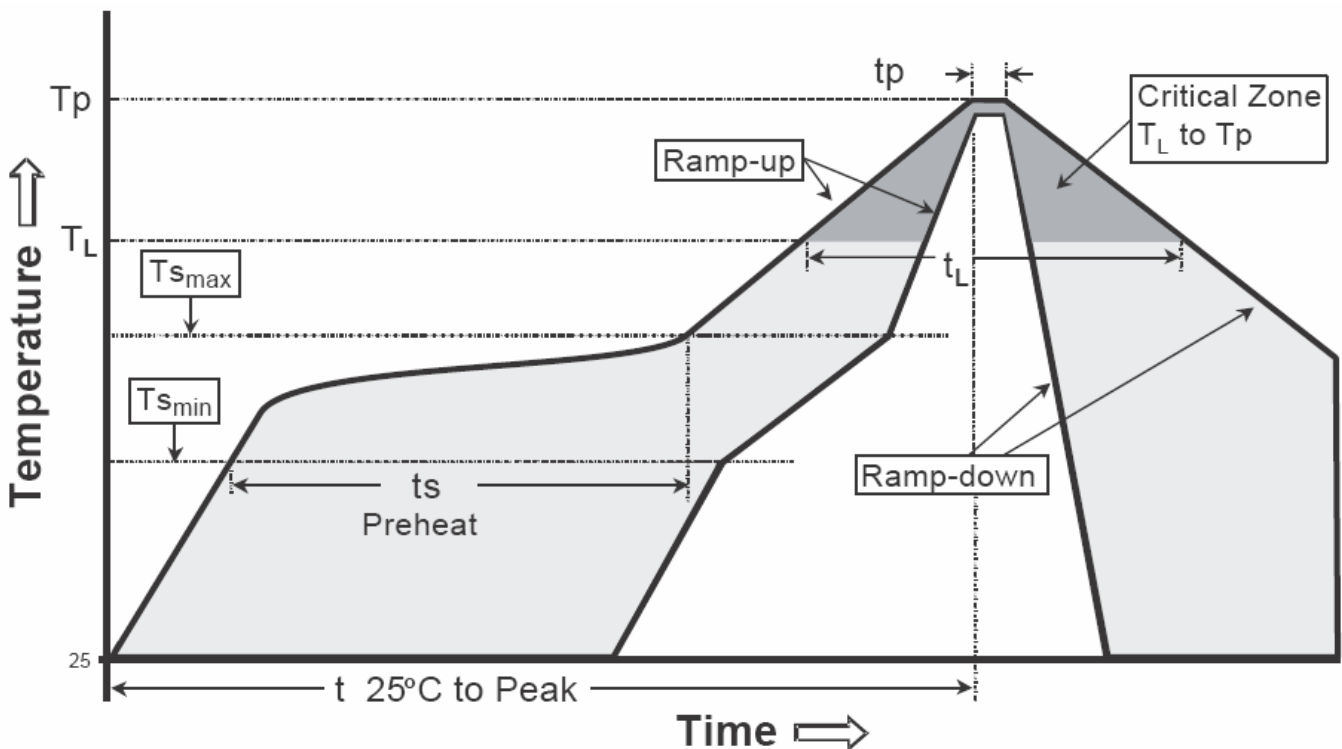
Notes:

1. 10 sprocket hole pitch cumulative tolerance ± 0.2 .
2. Camber not to exceed 1mm in 100mm.
3. Material: Conductive Black Advantek Polystyrene.
4. A_o & B_o measured on a plane 0.3mm above the bottom of the pocket.
5. K_o measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

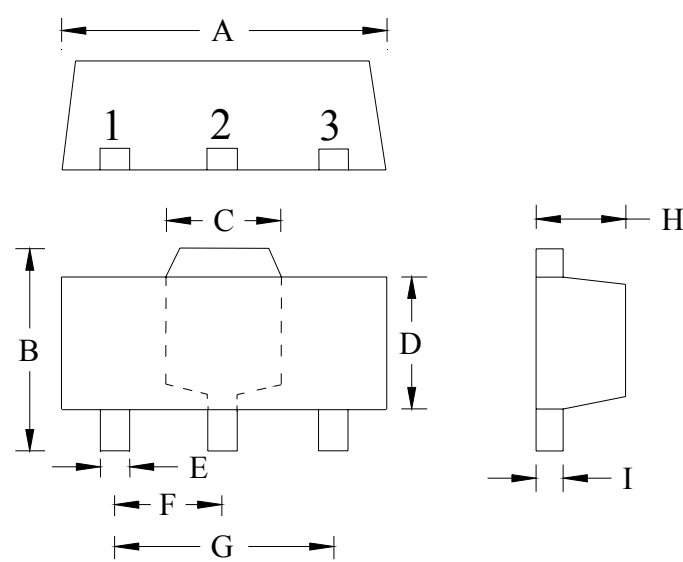
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (Tl)	183°C	217°C
- Time (tl)	60-150 seconds	60-150 seconds
Peak Temperature(Tp)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

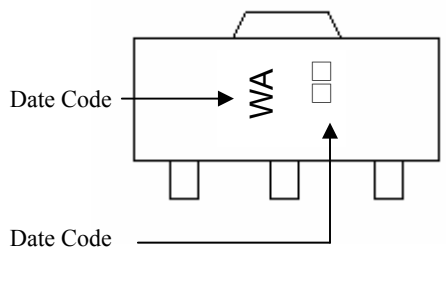
Note : All temperatures refer to topside of the package, measured on the package body surface.

SOT-89 Dimension



The diagram shows three views of the SOT-89 package: a top view with dimensions A, B, C, E, F, and G; a side view with dimensions D and H; and a perspective view with dimension I. The top view labels the three leads as 1, 2, and 3.

Marking:



The marking diagram shows a rectangular package with three leads. The top surface has a date code 'WA' and a small square symbol. Arrows point from the text 'Date Code' to these two features.

Style: Pin 1. Base 2. Collector 3. Emitter

3-Lead SOT-89 Plastic
 Surface Mounted Package
 CYStek Package Code: M3

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1732	0.1811	4.40	4.60	F	0.0591	TYP	1.50	TYP
B	0.1551	0.1673	3.94	4.25	G	0.1181	TYP	3.00	TYP
C	0.0610	REF	1.55	REF	H	0.0551	0.0630	1.40	1.60
D	0.0906	0.1024	2.30	2.60	I	0.0138	0.0173	0.35	0.44
E	0.0126	0.0205	0.32	0.52					

Notes: 1. Controlling dimension: millimeters.
 2. Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3. If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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