

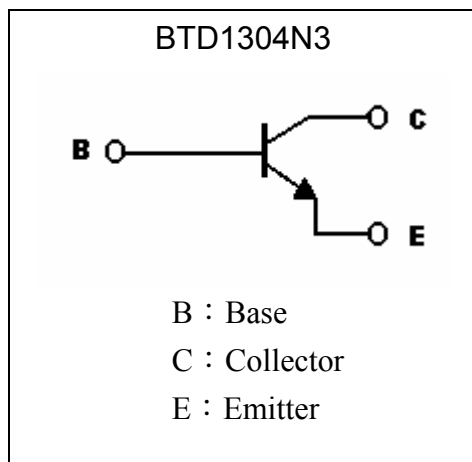
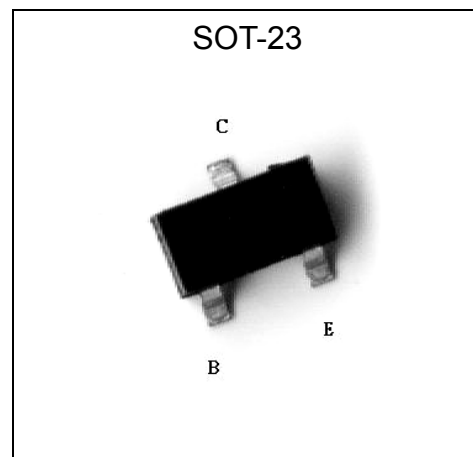
**NPN Epitaxial Planar Transistor
 AUDIO MUTING APPLICATION**

BTD1304N3

BV_{CEO}	20V
I_C	500mA
$R_{CE(SAT)}$	0.3 Ω (typ)

Features

- High Emitter-Base voltage, $V_{EBO}=12V(\text{min})$.
- High reverse h_{FE} , reverse $h_{FE}=20(\text{min.}) @V_{CE}=2V, I_C=4mA$.
- Low On-resistance, $R_{on}=0.6 \Omega (\text{max})@I_B=1mA$.
- Pb-free and halogen-free package.

Symbol

Outline

Absolute Maximum Ratings ($T_a=25^\circ\text{C}$)

Parameter	Symbol	Limit	Unit
Collector-Base Voltage	V_{CB0}	50	V
Collector-Emitter Voltage	V_{CEO}	20	V
Emitter-Base Voltage	V_{EBO}	12	V
Collector Current	I_C	500	mA
Base Current	I_B	50	mA
Power Dissipation	P_D	225	mW
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	556	$^\circ\text{C}/\text{W}$
Junction Temperature	T_j	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55~+150	$^\circ\text{C}$

**Characteristics (Ta=25°C)**

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV _{CB0}	50	-	-	V	I _C =100μA, I _E =0
BV _{CE0}	20	-	-	V	I _C =1mA, I _B =0
BV _{EB0}	12	-	-	V	I _E =10μA, I _C =0
I _{CB0}	-	-	100	nA	V _{CB} =40V, I _E =0
I _{EB0}	-	-	100	nA	V _{EB} =12V, I _C =0
*V _{CE(sat)}	-	34	100	mV	I _C =100mA, I _B =10mA
*V _{CE(sat)}	-	0.15	0.3	V	I _C =500mA, I _B =20mA
*R _{CE(sat)}	-	0.3	0.6	Ω	I _C =500mA, I _B =20mA
*V _{BE(sat)}	-	0.67	1	V	I _C =100mA, I _B =10mA
*h _{FE1} (FOR)	200	-	800	-	V _{CE} =2V, I _C =4mA
*h _{FE2} (FOR)	400	-	-	-	V _{CE} =3V, I _C =100mA
*h _{FE 3} (REV)	20	-	-	-	V _{CE} =2V, I _C =4mA
f _T	-	250	-	MHz	V _{CE} =10V, I _C =50mA, f=100MHz
Cob	-	10	-	pF	V _{CB} =10V, f=1MHz
Ron	-	-	0.6	Ω	Vin=0.3V, I _B =1mA, f=1KHz

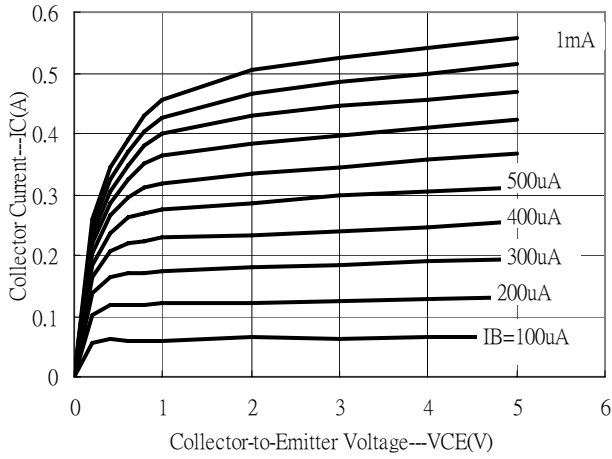
*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

Ordering Information

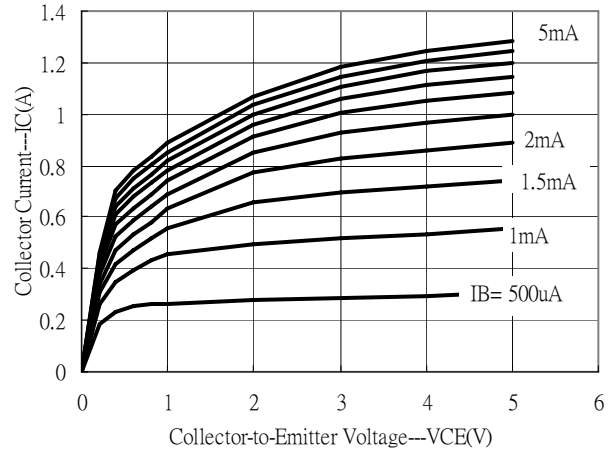
Device	Package	Shipping	Marking
BTD1304N3	SOT-23 (Pb-free and halogen-free package)	3000 pcs / Tape & Reel	MAX

Typical Characteristics

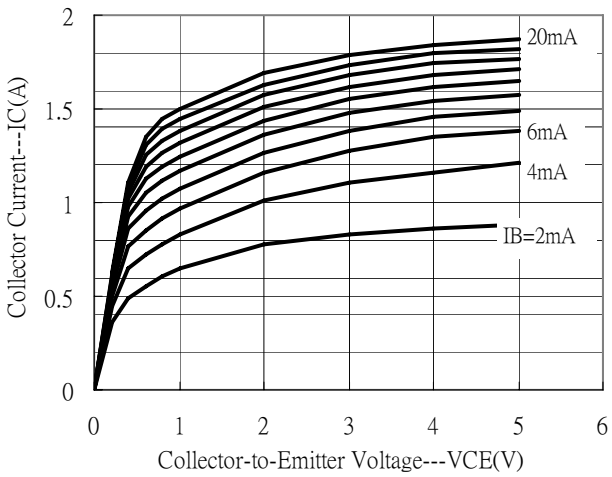
Emitter Grounded Output Characteristics



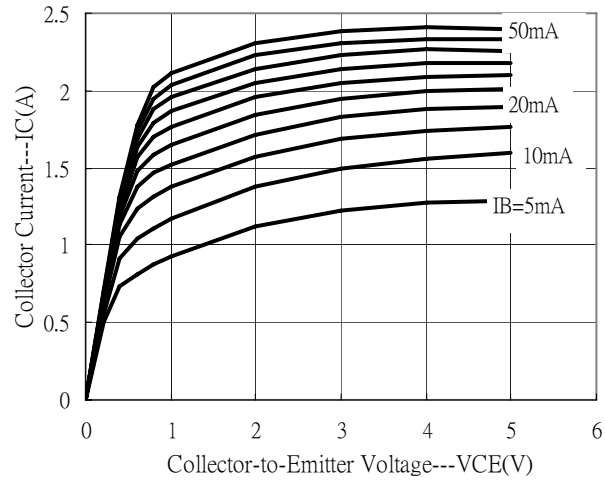
Emitter Grounded Output Characteristics



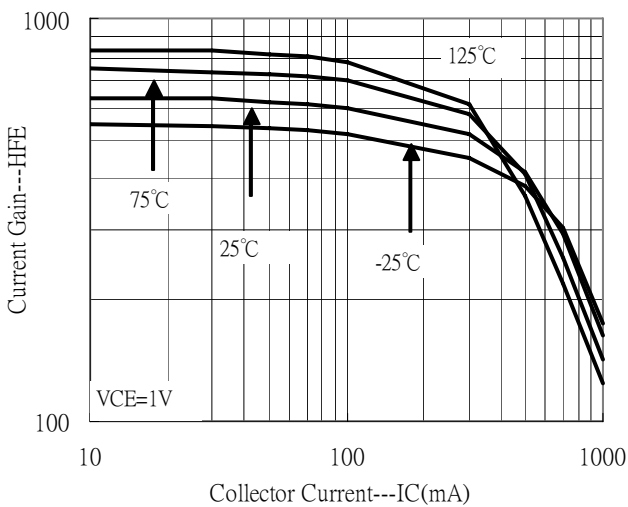
Emitter Grounded Output Characteristics



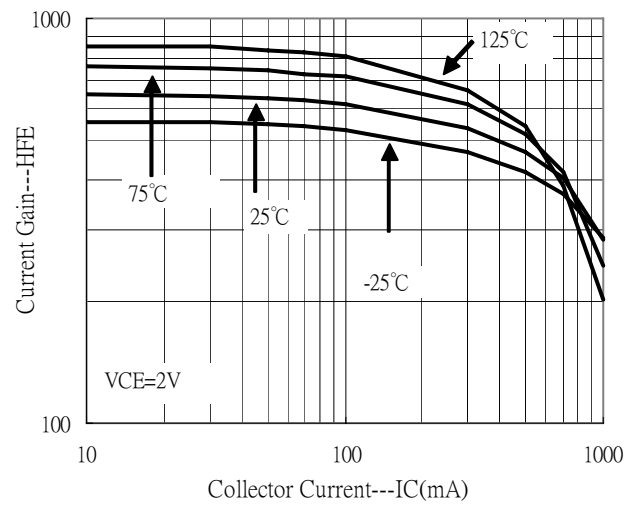
Emitter Grounded Output Characteristics



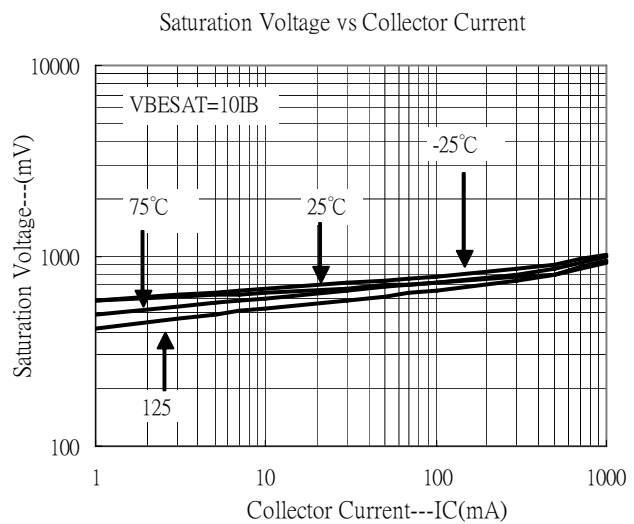
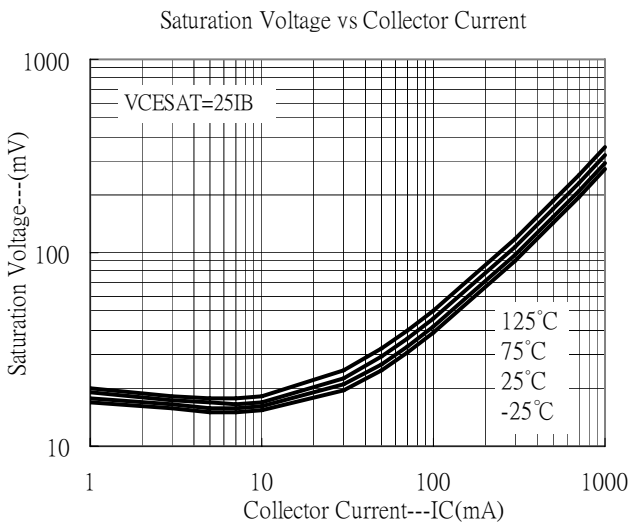
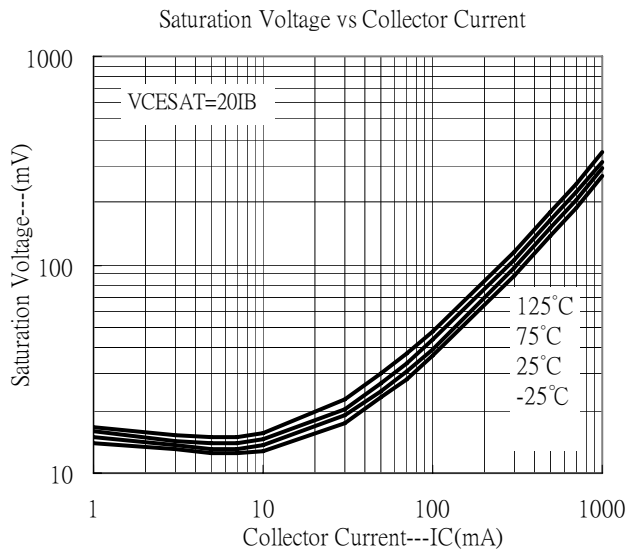
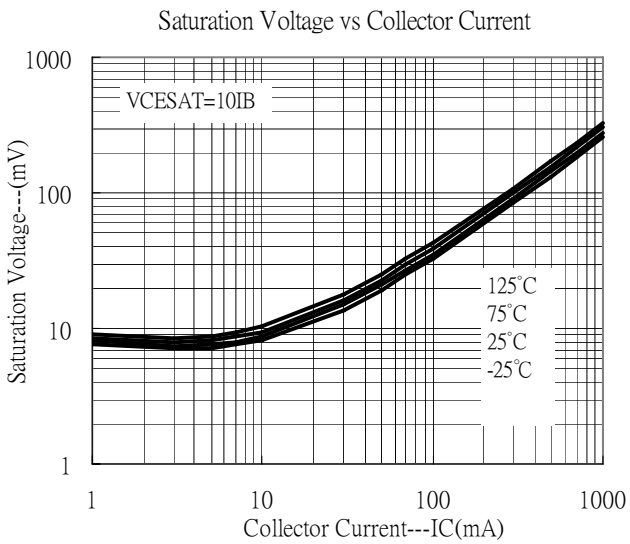
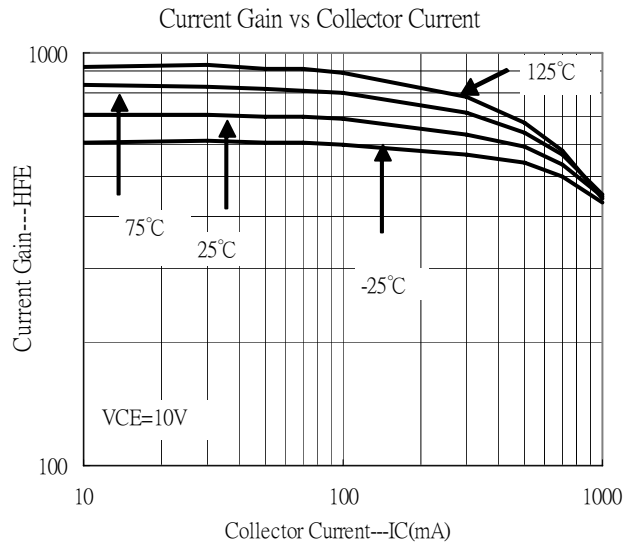
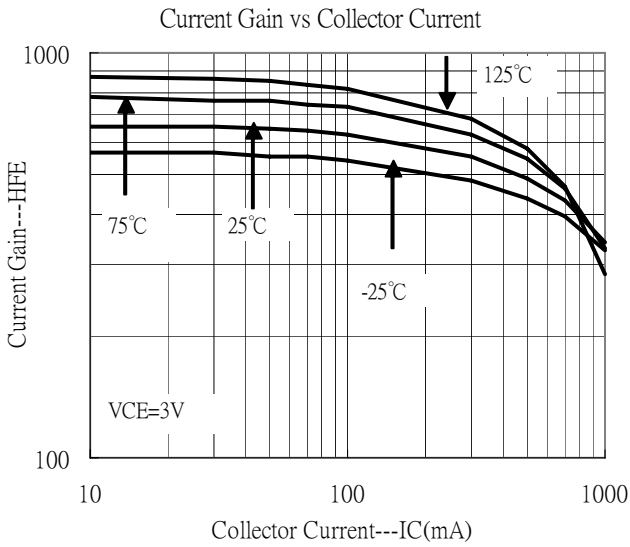
Current Gain vs Collector Current



Current Gain vs Collector Current

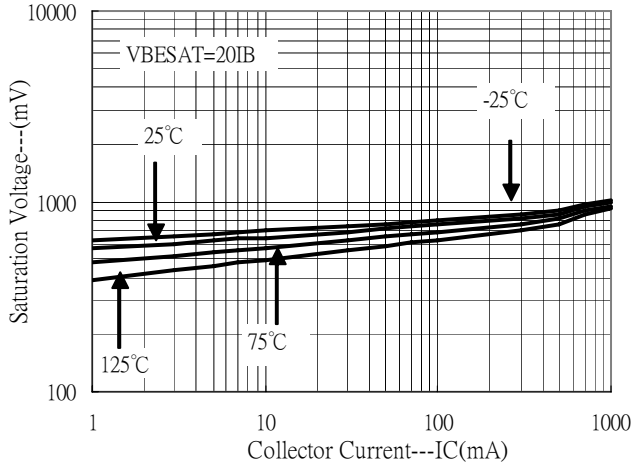


Typical Characteristics(Cont.)

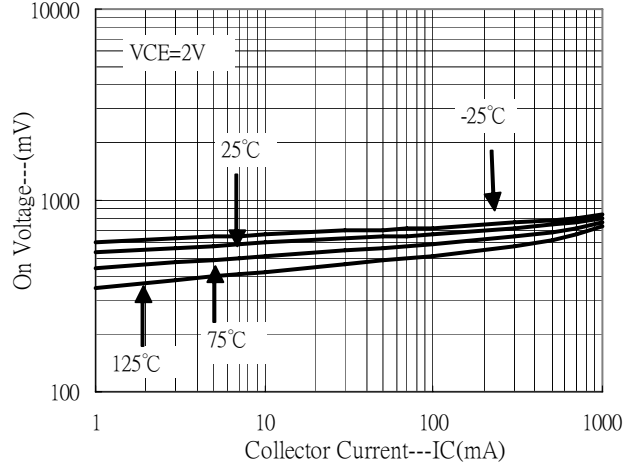


Typical Characteristics(Cont.)

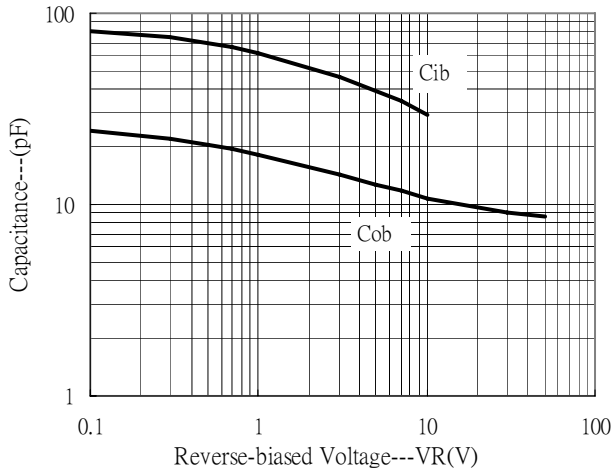
Saturation Voltage vs Collector Current



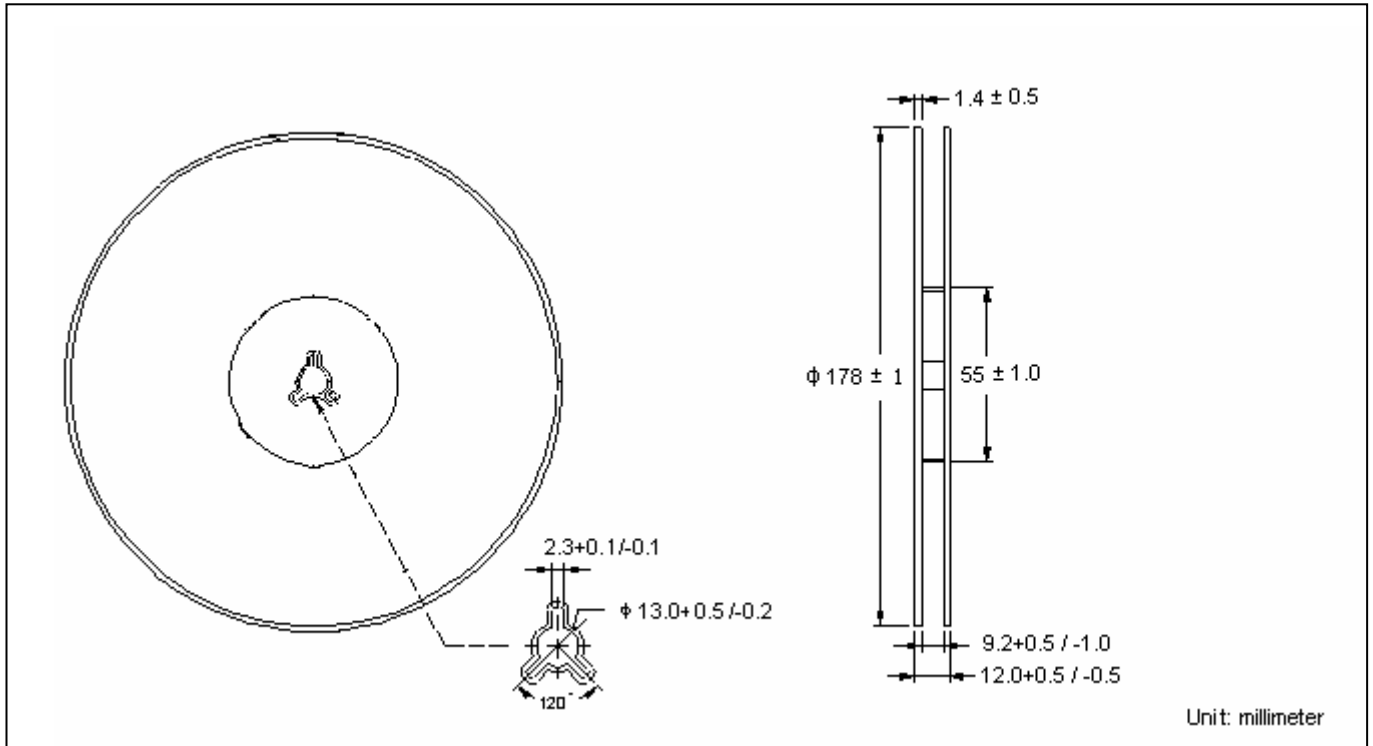
On Voltage vs Collector Current



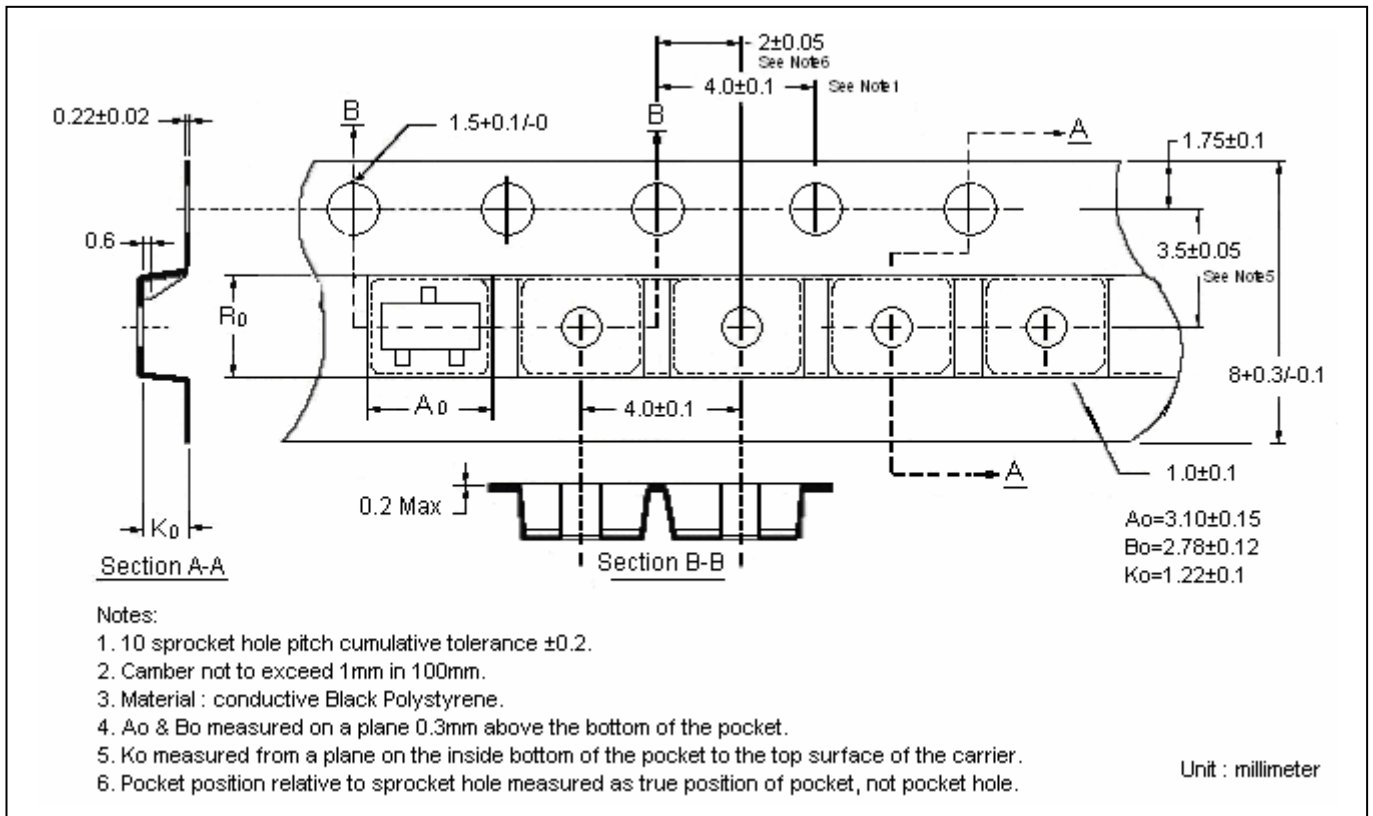
Capacitance vs Reverse-biased Voltage



Reel Dimension



Carrier Tape Dimension

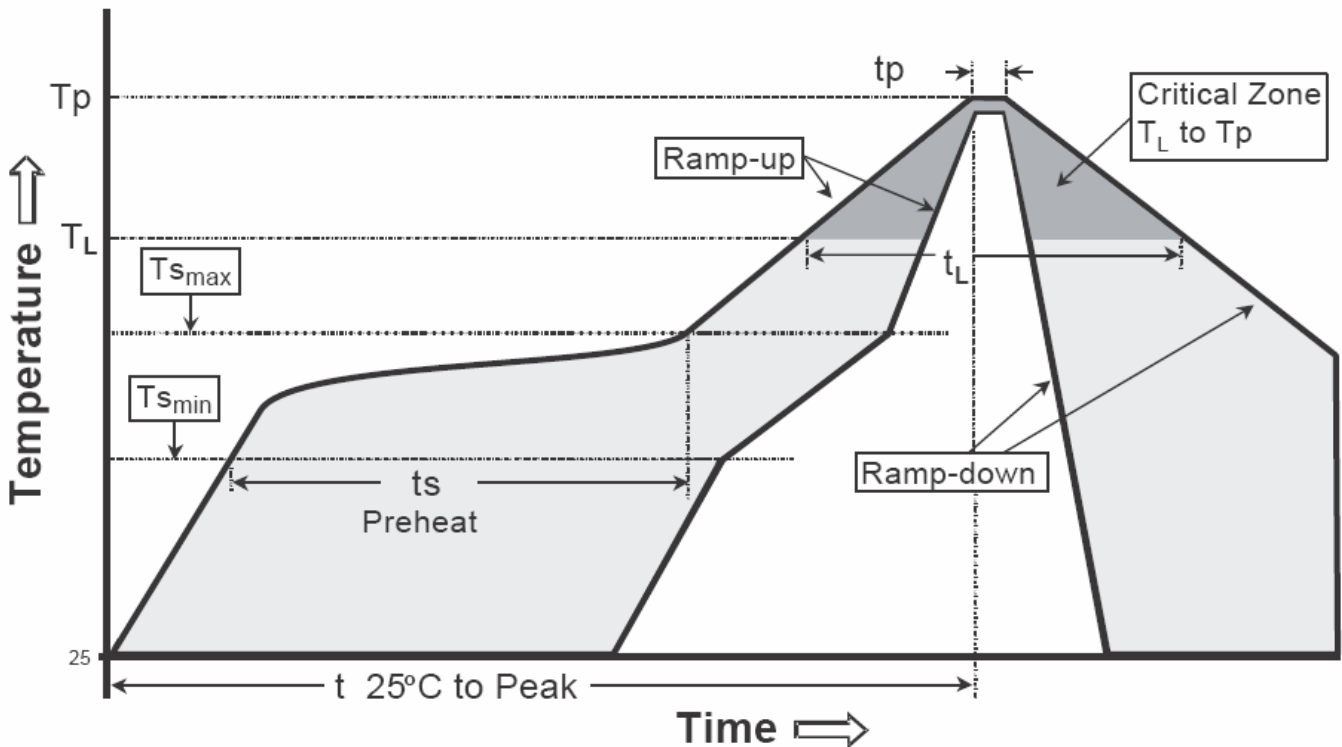


Notes:

1. 10 sprocket hole pitch cumulative tolerance ± 0.2 .
2. Camber not to exceed 1mm in 100mm.
3. Material : conductive Black Polystyrene.
4. A_0 & B_0 measured on a plane 0.3mm above the bottom of the pocket.
5. K_0 measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Recommended wave soldering condition

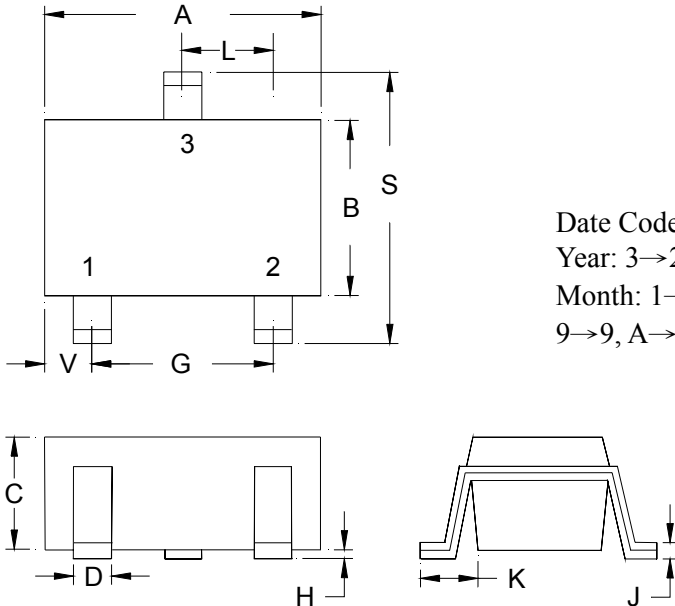
Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

Recommended temperature profile for IR reflow


Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _p)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

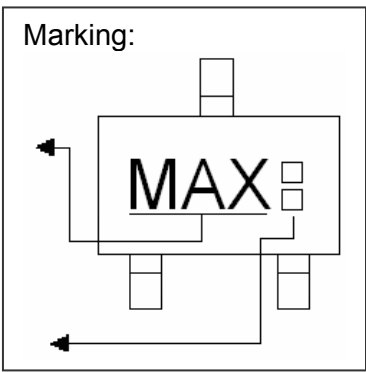
Note : All temperatures refer to topside of the package, measured on the package body surface.

SOT-23 Dimension



The diagram shows three views of the SOT-23 package: a top view with dimensions A, L, B, S, 1, 2, 3, V, and G; a side view with dimensions C, D, and H; and a perspective view with dimensions K and J. The top view labels 1, 2, and 3 correspond to the base, emitter, and collector pins respectively.

Marking:



The marking diagram shows a rectangular package with the letters "MAX" printed on the top surface. Arrows indicate the locations of the three leads.

Product Code

Date Code: Year+Month
 Year: 3→2003, 4→2004
 Month: 1→1, 2→2, . . .
 9→9, A→10, B→11, C→12

3-Lead SOT-23 Plastic Surface Mounted Package
 CYStek Package Code: N3

Style : Pin 1.Base 2.Emitter 3.Collector

*:Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1102	0.1204	2.80	3.04	J	0.0034	0.0070	0.085	0.177
B	0.0472	0.0630	1.20	1.60	K	0.0128	0.0266	0.32	0.67
C	0.0335	0.0512	0.89	1.30	L	0.0335	0.0453	0.85	1.15
D	0.0118	0.0197	0.30	0.50	S	0.0830	0.1083	2.10	2.75
G	0.0669	0.0910	1.70	2.30	V	0.0098	0.0256	0.25	0.65
H	0.0005	0.0040	0.013	0.10					

- Notes :** 1.Controlling dimension : millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material :

- Lead : Pure tin plated.
- Mold Compound : Epoxy resin family, flammability solid burning class:UL94V-0.

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.