

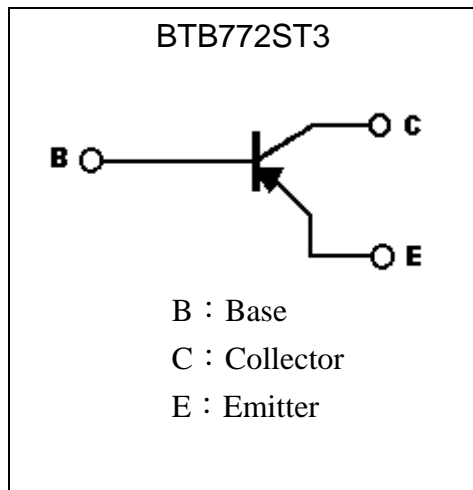
Low Vcesat PNP Epitaxial Planar Transistor

BTB772ST3

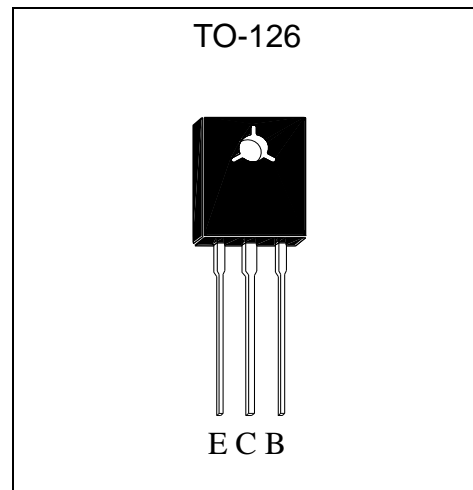
Features

- Low VCE(sat), typically -0.45 V at IC / IB = -2A / -0.2A
- Excellent current gain characteristics
- Pb-free lead plating and halogen-free package

Symbol

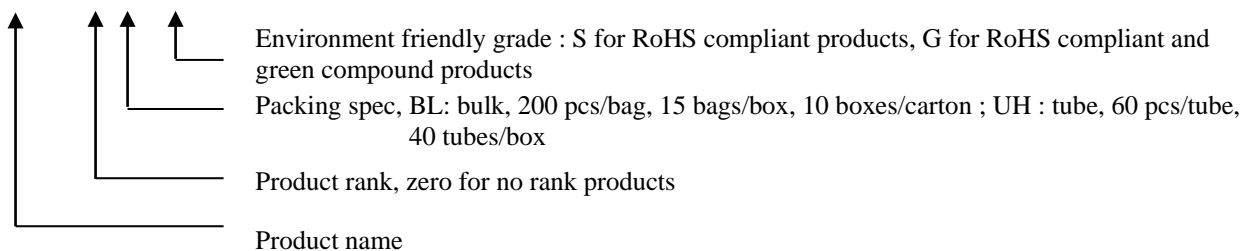


Outline



Ordering Information

Device	Package	Shipping
BTB772ST3-P-BL-X	TO-126 (Pb-free lead plating and halogen-free package)	200 pcs / bag, 3,000 pcs/box 30,000 pcs/carton
BTB772ST3-P-UH-X		60 pcs/ tube, 40 tubes/box



**Absolute Maximum Ratings** (Ta=25°C)

Parameter	Symbol	Limit	Unit
Collector-Base Voltage	V _{CBO}	-40	V
Collector-Emitter Voltage	V _{CEO}	-30	V
Emitter-Base Voltage	V _{EBO}	-5	V
Collector Current	I _C (DC)	-2	A
	I _C (pulse)	-5 *1	A
Power Dissipation	P _d (Ta=25°C)	1	W
	P _d (Tc=25°C)	10	
Junction Temperature	T _j	150	°C
Storage Temperature	T _{stg}	-55~+150	°C

Note : *1. Single Pulse Pw ≤ 300μs, Duty ≤ 2%.

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	R _{th,j-c}	12.5	°C/W
Thermal Resistance, Junction-to-ambient, max	R _{th,j-a}	125	°C/W

Characteristics (Ta=25°C)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV _{CBO}	-40	-	-	V	I _C =-50μA, I _E =0
BV _{CEO}	-30	-	-	V	I _C =-1mA, I _B =0
BV _{EBO}	-5	-	-	V	I _E =-50μA, I _C =0
I _{CBO}	-	-	-1	μA	V _{CB} =-30V, I _E =0
I _{EBO}	-	-	-1	μA	V _{EB} =-5V, I _C =0
*V _{CE(sat)}	-	-0.45	-0.6	V	I _C =-2A, I _B =-0.2A
*V _{BE(sat)}	-	-1	-1.5	V	I _C =-2A, I _B =-0.2A
*h _{FE} 1	120	-	-	-	V _{CE} =-2V, I _C =-20mA
*h _{FE} 2	180	-	390	-	V _{CE} =-2V, I _C =-500mA
f _T	-	80	-	MHz	V _{CE} =-5V, I _E =-0.1A, f=100MHz
C _{ob}	-	55	-	pF	V _{CB} =-10V, f=1MHz

*Pulse Test : Pulse Width ≤ 380μs, Duty Cycle ≤ 2%

Classification Of h_{FE} 2

Rank	P
Range	180~390

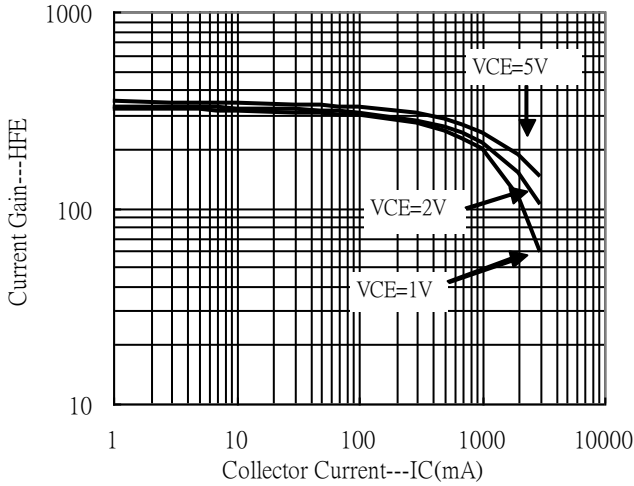
Recommended Storage Condition:

Temperature : 10~ 35 °C

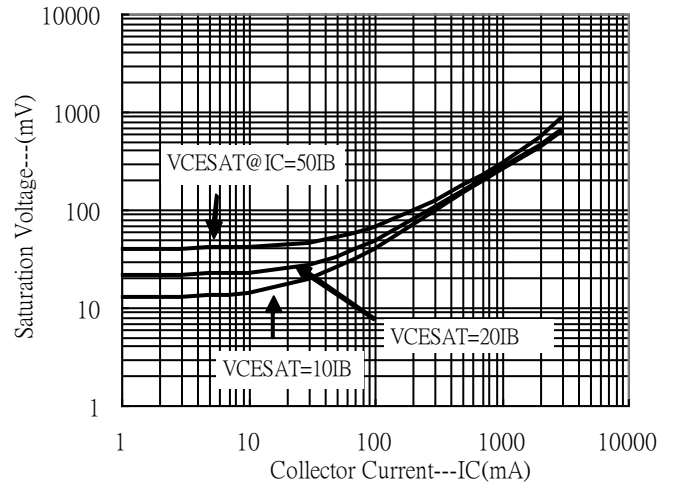
Humidity : 30~ 60% RH

Typical Characteristics

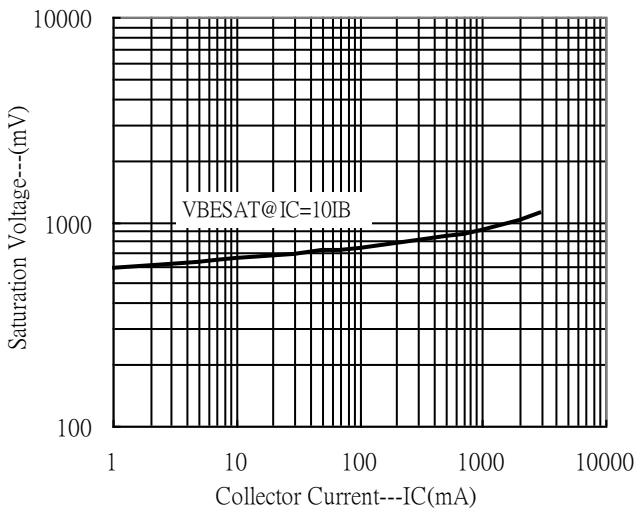
Current Gain vs Collector Current



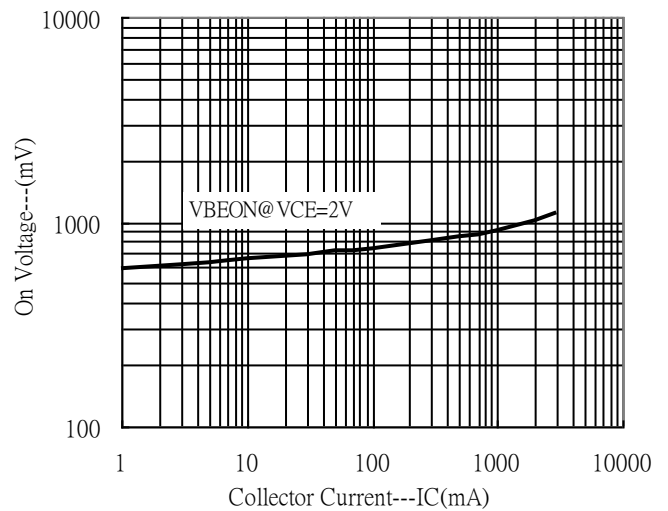
Saturation Voltage vs Collector Current



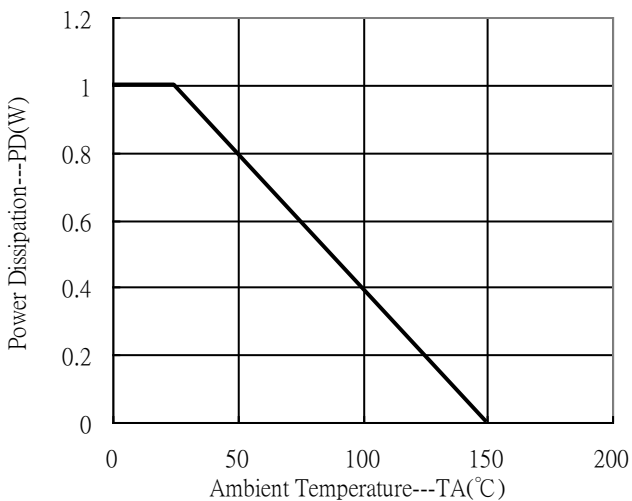
Saturation Voltage vs Collector Current



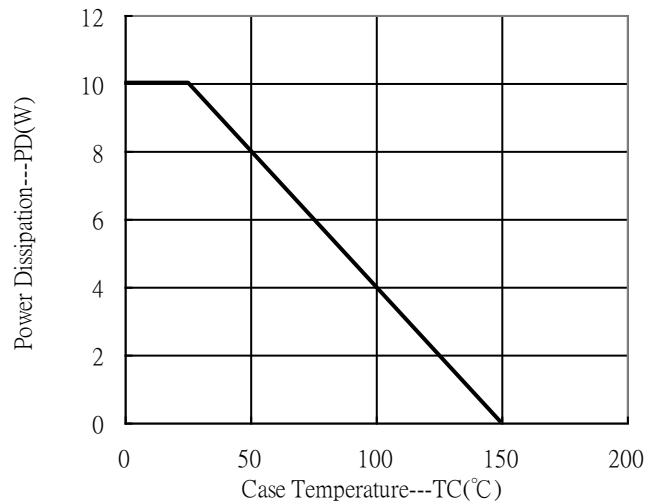
On Voltage vs Collector Current



Power Derating Curve



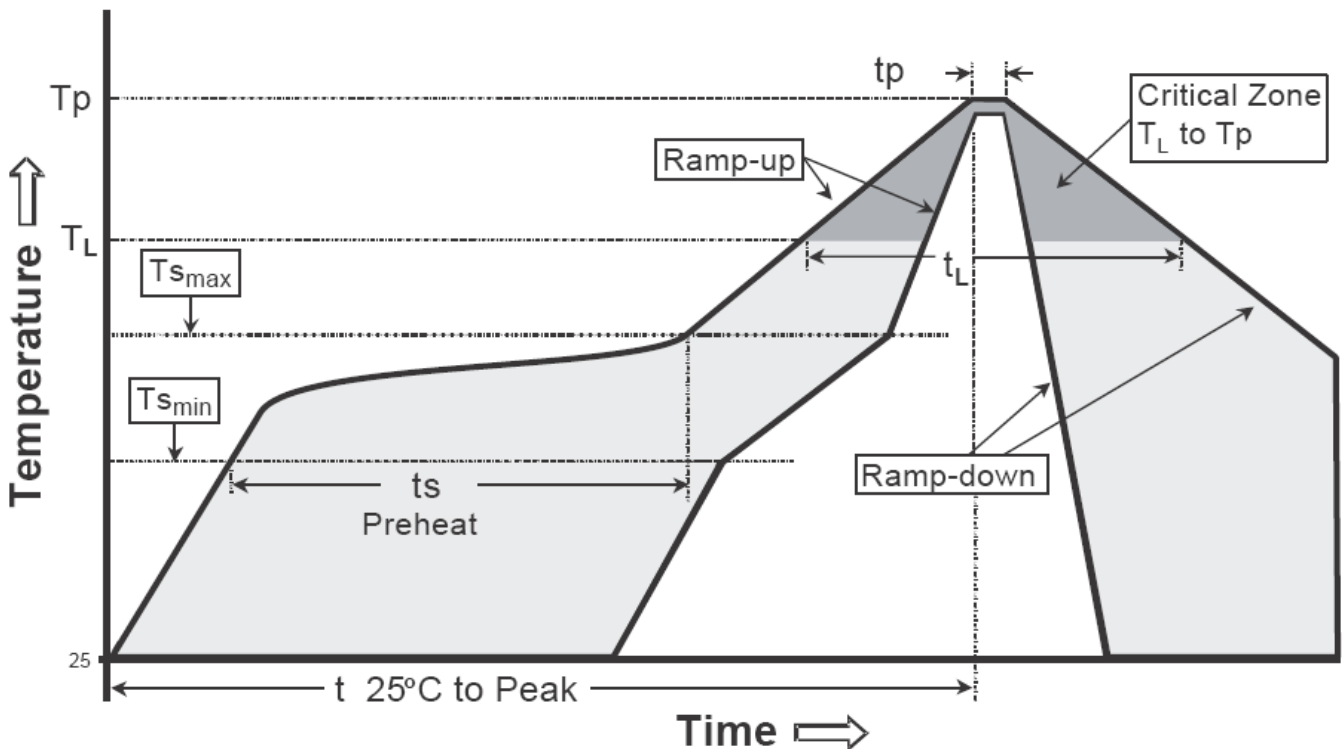
Power Derating Curve



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

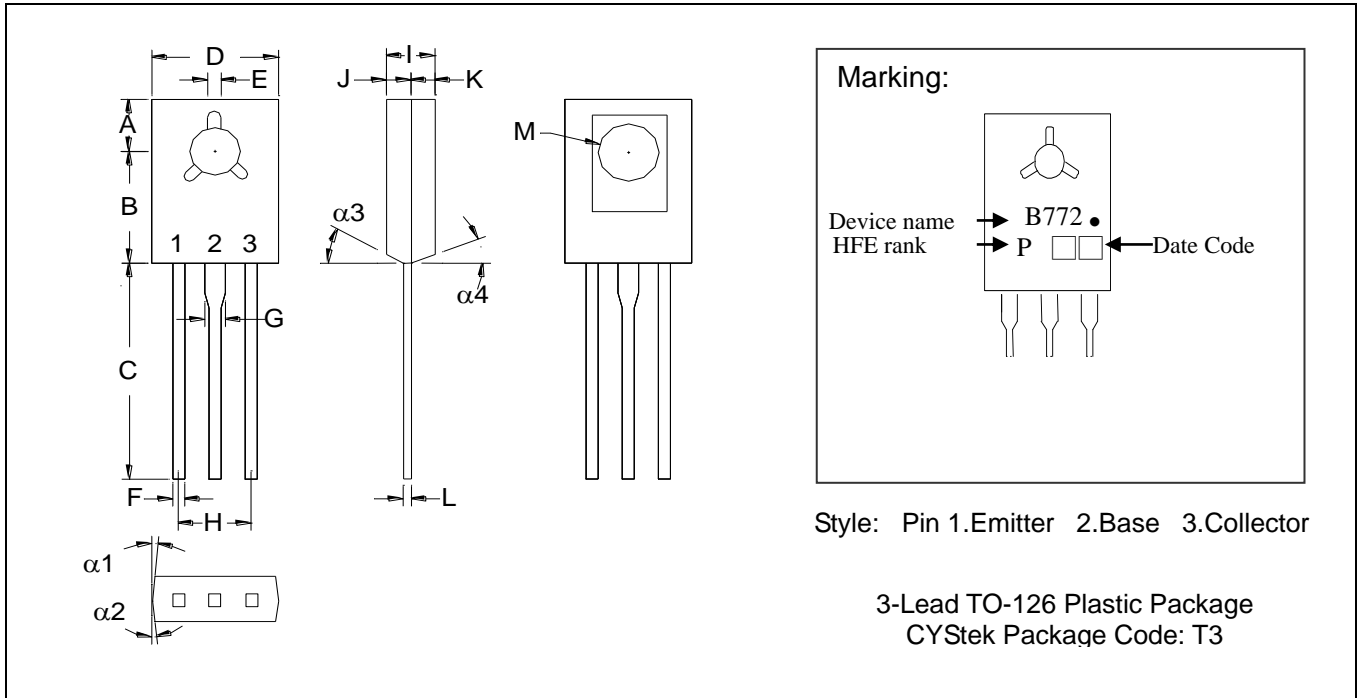
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-126 Dimension



*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
α_1	-	*3°	-	*3°	F	0.0280	0.0319	0.71	0.81
α_2	-	*3°	-	*3°	G	0.0480	0.0520	1.22	1.32
α_3	-	*3°	-	*3°	H	0.1709	0.1890	4.34	4.80
α_4	-	*3°	-	*3°	I	0.0950	0.1050	2.41	2.66
A	0.1500	0.1539	3.81	3.91	J	0.0450	0.0550	1.14	1.39
B	0.2752	0.2791	6.99	7.09	K	0.0450	0.0550	1.14	1.39
C	0.5315	0.6102	13.50	15.50	L	-	*0.0217	-	*0.55
D	0.2854	0.3039	7.52	7.72	M	0.1378	0.1520	3.50	3.86
E	0.0374	0.0413	0.95	1.05					

- Notes:**
- Controlling dimension: millimeters.
 - Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 - If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: KFC; tin plating
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.