

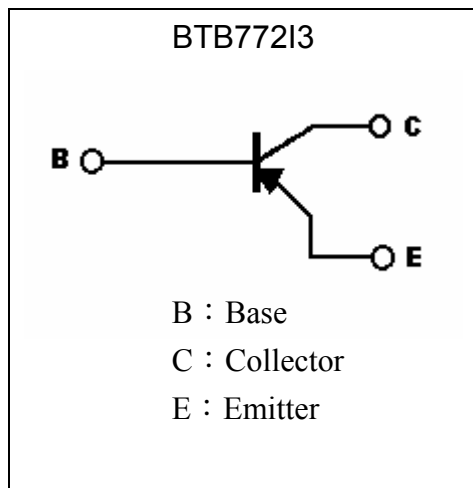
**Low Vcesat PNP Epitaxial Planar Transistor**

# BTB772I3

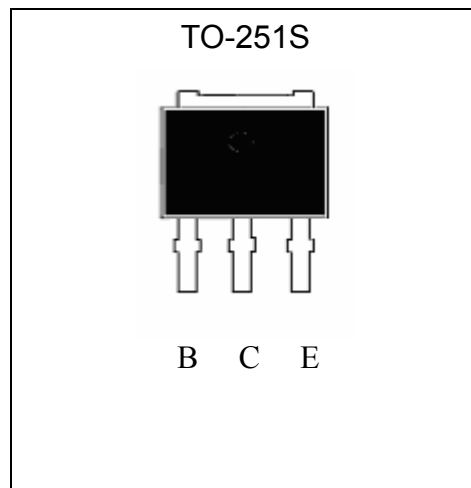
## Features

- Low VCE(sat), typically -0.45 V at IC / IB = -2A / -0.2A
- Excellent current gain characteristics
- Complementary to BTD882I3
- Pb-free lead plating and halogen-free package

## Symbol

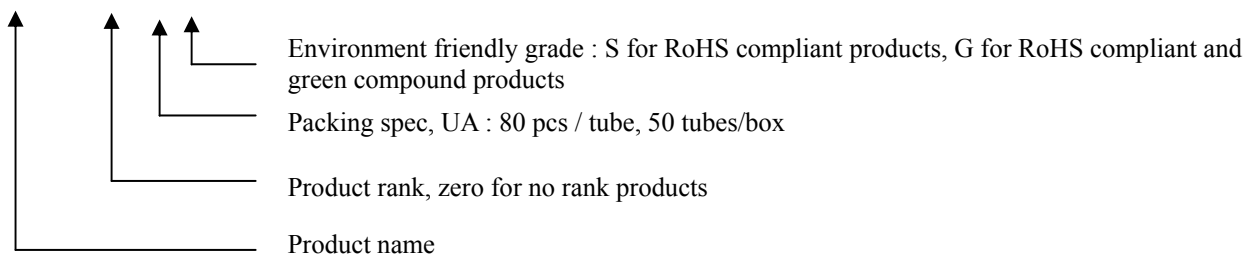


## Outline



## Ordering Information

Device	Package	Shipping
BTB772I3-X-UA-G	TO-251S (Pb-free lead plating and halogen-free package)	80 pcs/tube, 50 tubes/box



**Absolute Maximum Ratings** (Ta=25°C)

Parameter	Symbol	Limit	Unit
Collector-Base Voltage	V <sub>CBO</sub>	-40	V
Collector-Emitter Voltage	V <sub>CEO</sub>	-30	V
Emitter-Base Voltage	V <sub>EBO</sub>	-5	V
Collector Current	I <sub>C</sub> (DC)	-2	A
	I <sub>C</sub> (pulse)	-5 *1	A
Power Dissipation	Pd(Ta=25°C)	1	W
	Pd(Tc=25°C)	10	
Junction Temperature	T <sub>j</sub>	150	°C
Storage Temperature	T <sub>stg</sub>	-55~+150	°C

Note : \*1. Single Pulse Pw ≤ 350μs, Duty ≤ 2%.

**Characteristics** (Ta=25°C)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV <sub>CBO</sub>	-40	-	-	V	I <sub>C</sub> =-50μA, I <sub>E</sub> =0
BV <sub>CEO</sub>	-30	-	-	V	I <sub>C</sub> =-1mA, I <sub>B</sub> =0
BV <sub>EBO</sub>	-5	-	-	V	I <sub>E</sub> =-50μA, I <sub>C</sub> =0
I <sub>CBO</sub>	-	-	-1	μA	V <sub>CB</sub> =-30V, I <sub>E</sub> =0
I <sub>EBO</sub>	-	-	-1	μA	V <sub>EB</sub> =-5V, I <sub>C</sub> =0
*V <sub>CE(sat)</sub>	-	-0.45	-0.6	V	I <sub>C</sub> =-2A, I <sub>B</sub> =-0.2A
*V <sub>BE(sat)</sub>	-	-1	-1.5	V	I <sub>C</sub> =-2A, I <sub>B</sub> =-0.2A
*h <sub>FE</sub> 1	120	-	-	-	V <sub>CE</sub> =-2V, I <sub>C</sub> =-20mA
*h <sub>FE</sub> 2	180	-	500	-	V <sub>CE</sub> =-2V, I <sub>C</sub> =-500mA
f <sub>T</sub>	-	80	-	MHz	V <sub>CE</sub> =-5V, I <sub>E</sub> =-0.1A, f=100MHz
Cob	-	55	-	pF	V <sub>CB</sub> =-10V, f=1MHz

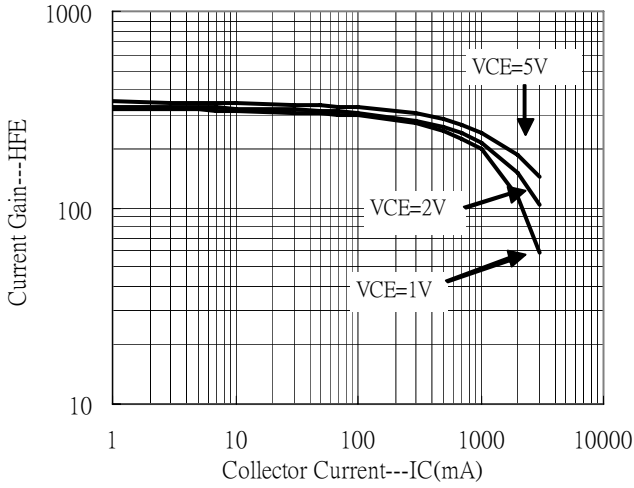
\*Pulse Test : Pulse Width ≤ 380μs, Duty Cycle ≤ 2%

**Classification Of hFE 2**

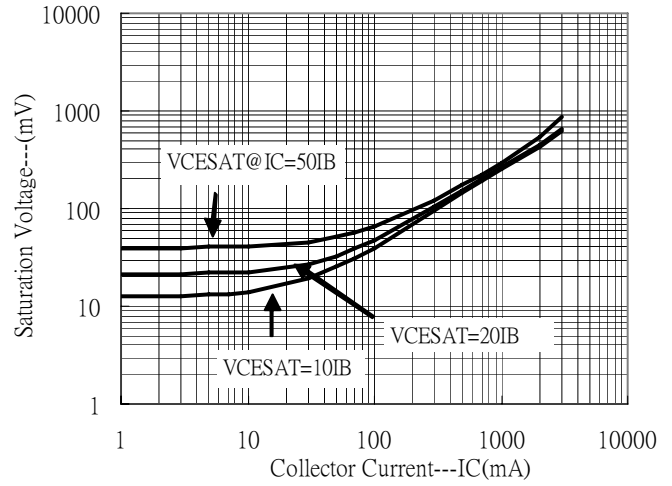
Rank	P	E
Range	180~390	250~500

**Characteristic Curves**

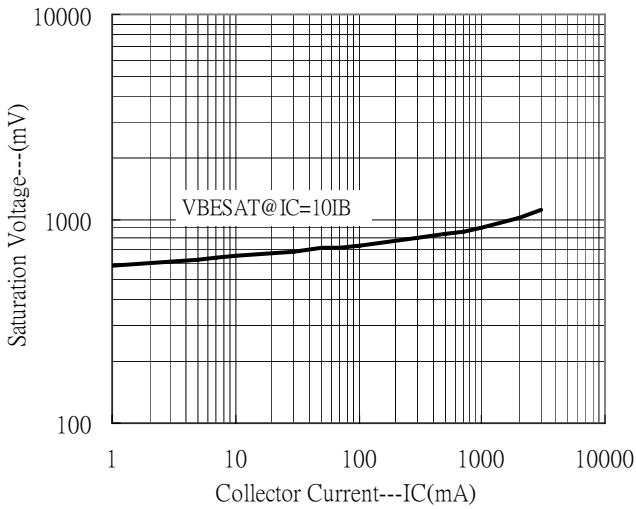
Current Gain vs Collector Current



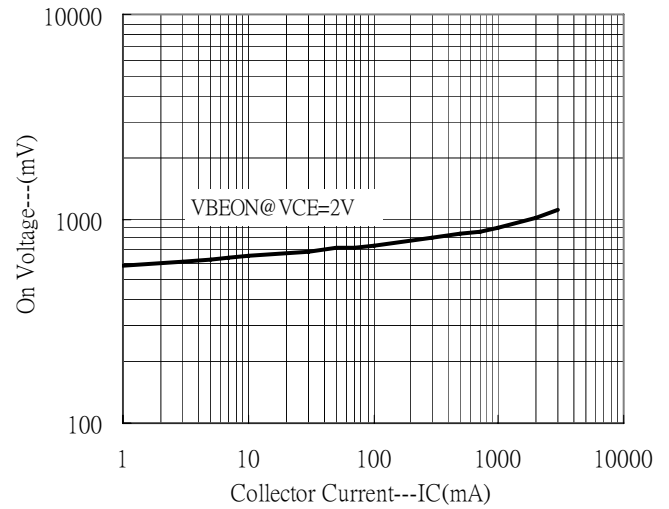
Saturation Voltage vs Collector Current



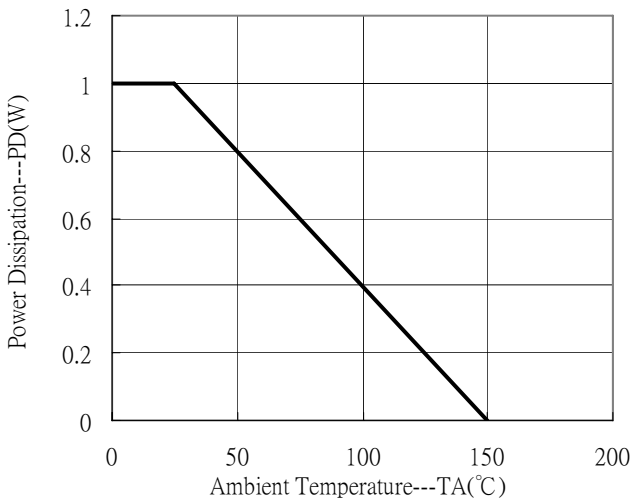
Saturation Voltage vs Collector Current



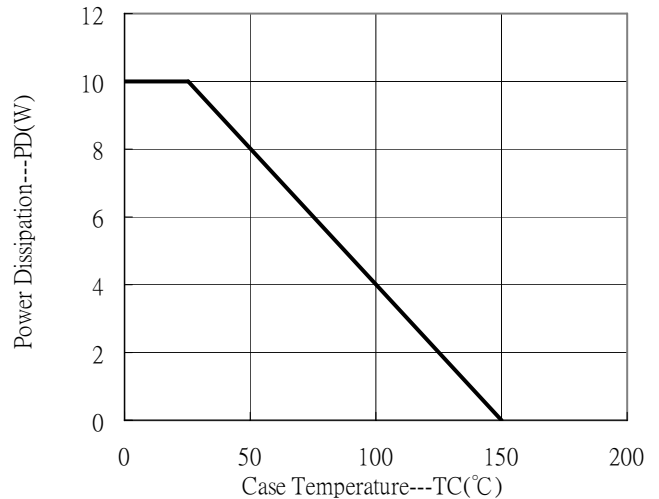
On Voltage vs Collector Current



Power Derating Curve



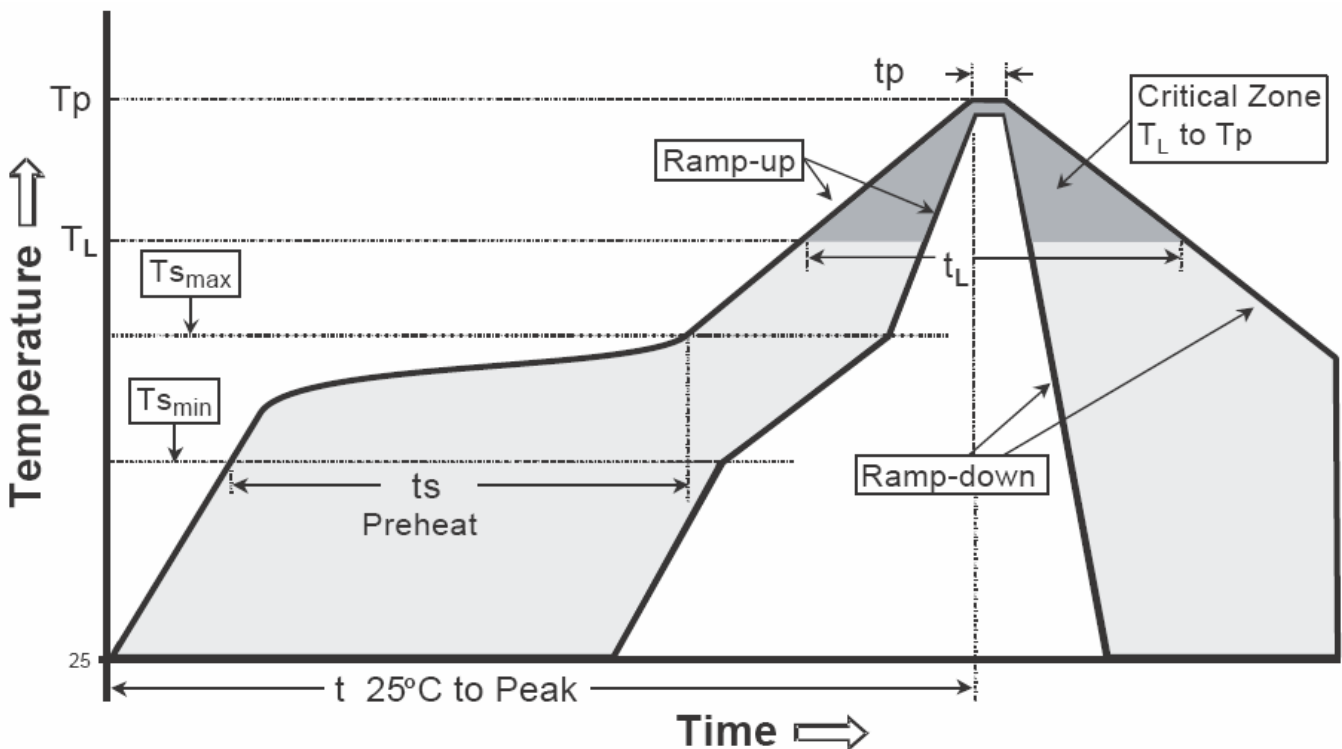
Power Derating Curve



**Recommended wave soldering condition**

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

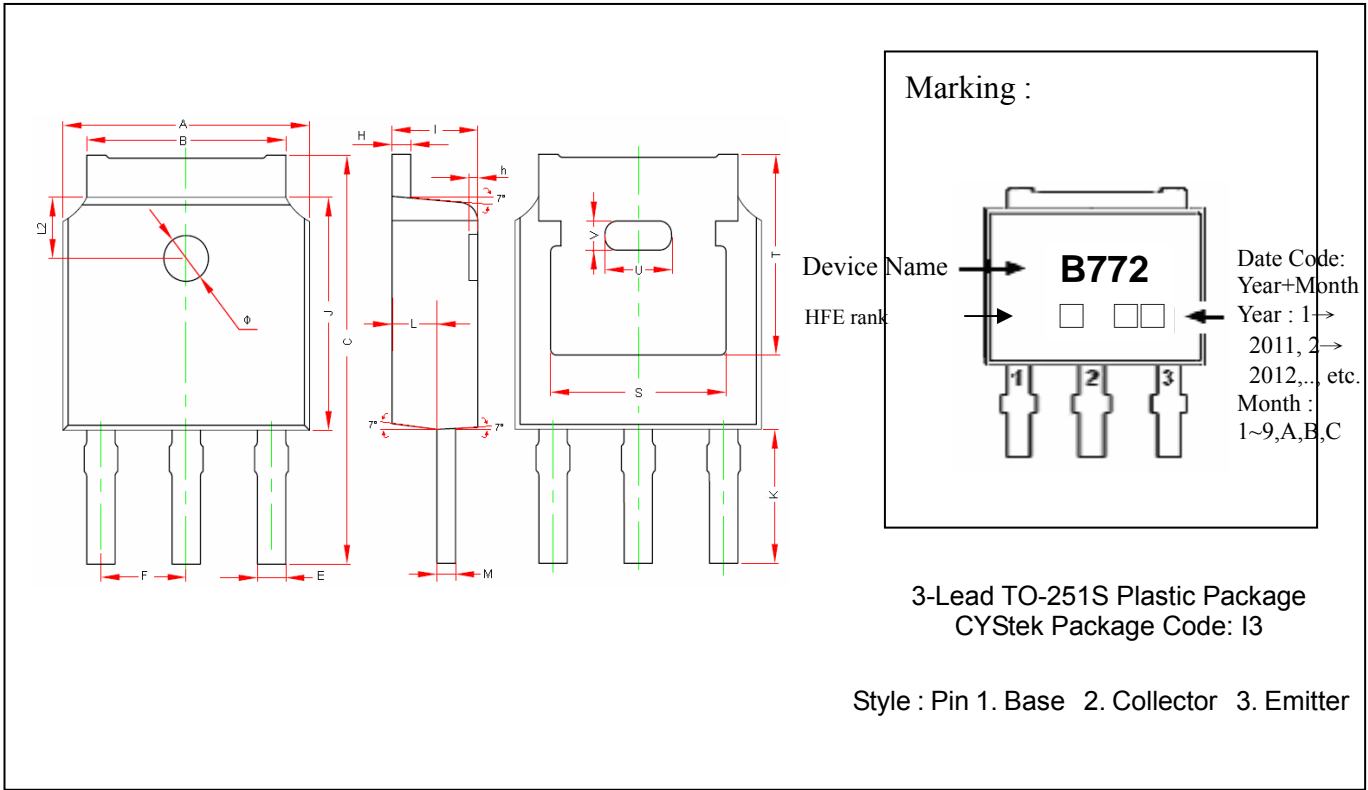
**Recommended temperature profile for IR reflow**



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (Tl)	183°C	217°C
- Time (tl)	60-150 seconds	60-150 seconds
Peak Temperature(Tp)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

**TO-251S Dimension**



**Marking :**

Device Name → **B772**      Date Code:  
 HFE rank →      Year+Month  
 Year : 1 → 2011, 2 → 2012,... etc.  
 Month : 1~9, A, B, C

3-Lead TO-251S Plastic Package  
 CYStek Package Code: I3

Style : Pin 1. Base 2. Collector 3. Emitter

\*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.256	0.264	6.500	6.700	K	0.138	REF	3.500	REF
B	0.201	0.215	5.100	5.460	L	0.036	0.046	0.910	1.110
C	0.409	0.433	10.400	11.000	L2	0.063	REF	1.600	REF
E	0.026	0.034	0.660	0.860	M	0.018	0.023	0.460	0.580
F	0.086	0.094	2.186	2.386	S	0.190	REF	4.830	REF
H	0.018	0.023	0.460	0.580	T	0.211	REF	5.350	REF
h	0.000	0.012	0.000	0.300	U	0.070	REF	1.780	REF
I	0.087	0.094	2.200	2.400	V	0.030	REF	0.760	REF
J	0.236	0.244	6.000	6.200	Φ	0.043	0.051	1.100	1.300

**Notes:** 1.Controlling dimension: inch.  
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.  
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

**Material:**

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

**Important Notice:**

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.