

Silicon PNP Epitaxial Planar Transistor

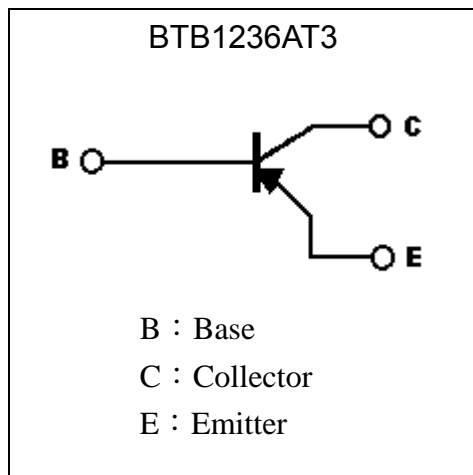
BTB1236AT3

BV_{CEO}	-160V
I_C	-1.5A

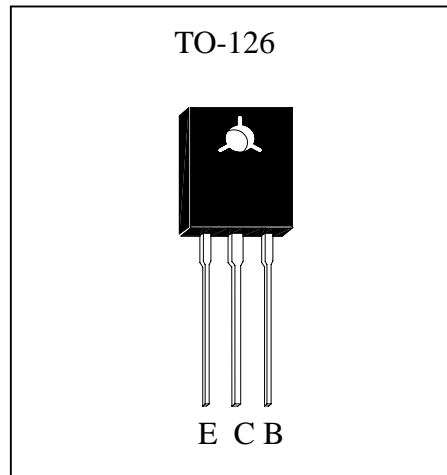
Description

- High BV_{CEO}
- High current capability
- Pb-free lead plating package

Symbol

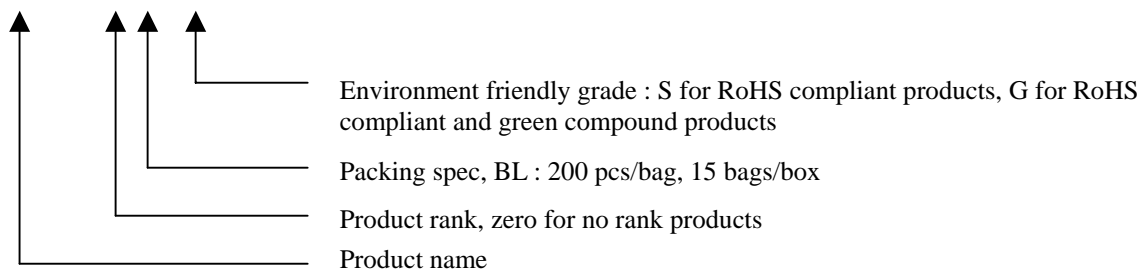


Outline



Ordering Information

Device	Package	Shipping
BTB1236AT3-0-BL-X	TO-126 (Pb-free lead plating package)	200 pcs / bag, 15 bags/box



**Absolute Maximum Ratings** ($T_a=25^{\circ}\text{C}$)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V_{CB0}	-180	V
Collector-Emitter Voltage	V_{CE0}	-160	V
Emitter-Base Voltage	V_{EB0}	-5	V
Collector Current (DC)	I_C	-1.5	A
Collector Current (Pulse)	I_{CP}	-3	A
Base Current	I_B	0.5	A
Power Dissipation @ $T_A=25^{\circ}\text{C}$	P_D	1	W
Power Dissipation @ $T_C=25^{\circ}\text{C}$		20	
Junction Temperature	T_j	150	$^{\circ}\text{C}$
Storage Temperature	T_{stg}	-55~+150	$^{\circ}\text{C}$

Characteristics ($T_a=25^{\circ}\text{C}$)

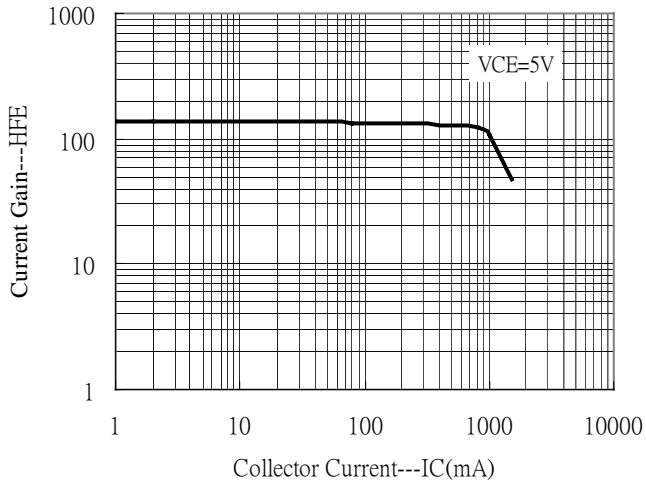
Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV_{CB0}	-180	-	-	V	$I_C=-50\mu\text{A}$, $I_E=0$
BV_{CE0}	-160	-	-	V	$I_C=-1\text{mA}$, $I_B=0$
BV_{EB0}	-5	-	-	V	$I_E=-50\mu\text{A}$, $I_C=0$
I_{CBO}	-	-	-1	μA	$V_{CB}=-160\text{V}$, $I_E=0$
I_{EB0}	-	-	-1	μA	$V_{EB}=-4\text{V}$, $I_C=0$
* $V_{CE(sat)}$	-	-0.24	-0.6	V	$I_C=-1\text{A}$, $I_B=-100\text{mA}$
* $R_{CE(sat)}$	-	0.24	0.6	Ω	$I_C=-1\text{A}$, $I_B=-100\text{mA}$
* $V_{BE(on)}$	-	-	-1.5	V	$V_{CE}=-5\text{V}$, $I_C=-150\text{mA}$
h_{FE1}	180	-	390	-	$V_{CE}=-5\text{V}$, $I_C=-100\text{mA}$
h_{FE2}	120	-	-	-	$V_{CE}=-5\text{V}$, $I_C=-500\text{mA}$
f_T	-	180	-	MHz	$V_{CE}=-5\text{V}$, $I_C=-150\text{mA}$
Cob	-	24	-	pF	$V_{CB}=-10\text{V}$, $I_E=0$, $f=1\text{MHz}$

*Pulse Test: Pulse Width $\leq 380\mu\text{s}$, Duty Cycle $\leq 2\%$

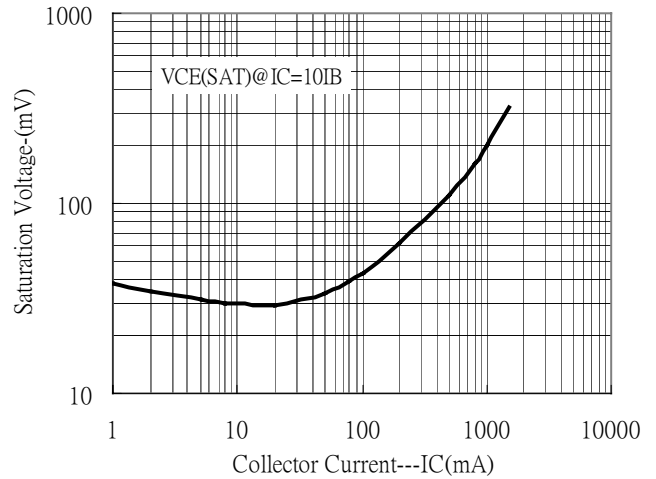


Typical Characteristics

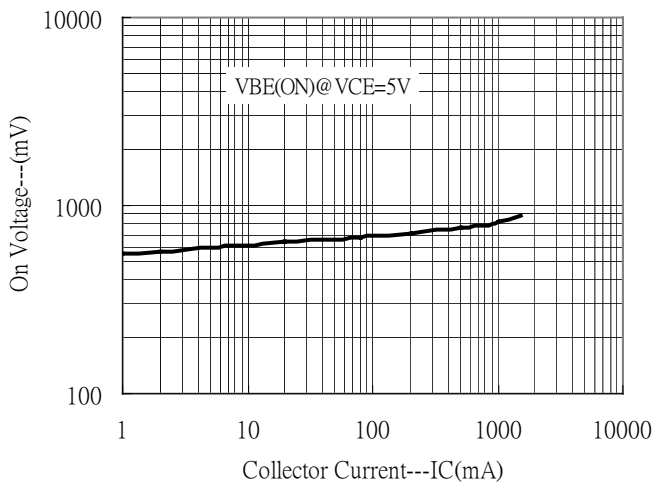
Current Gain vs Collector Current



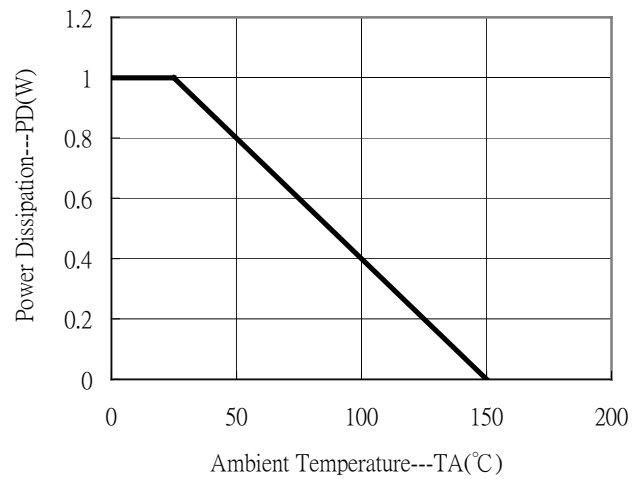
Saturation Voltage vs Collector Current



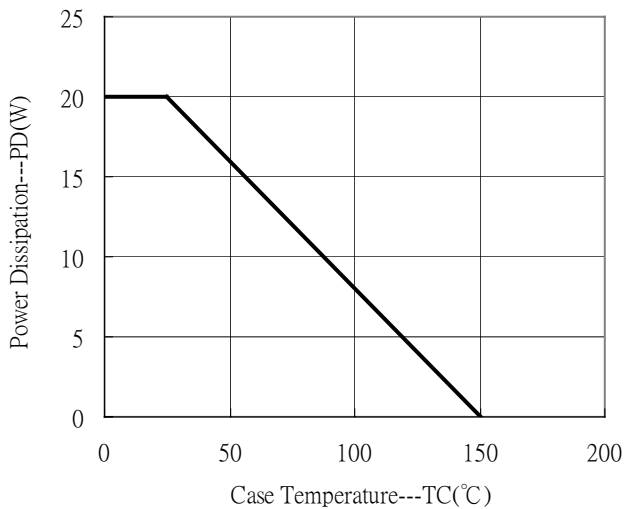
On Voltage vs Collector Current



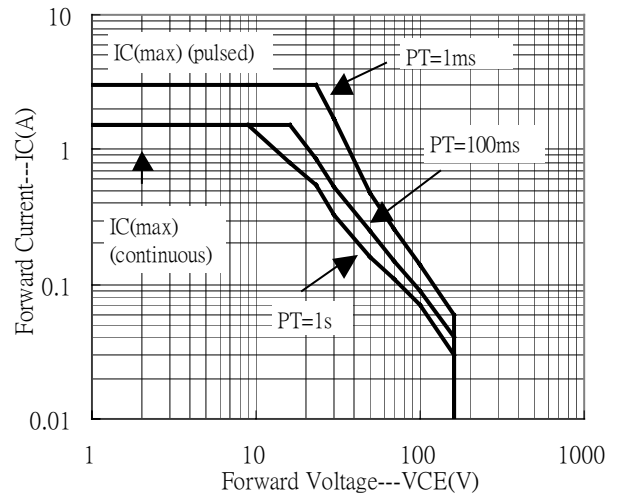
Power Derating Curve



Power Derating Curve



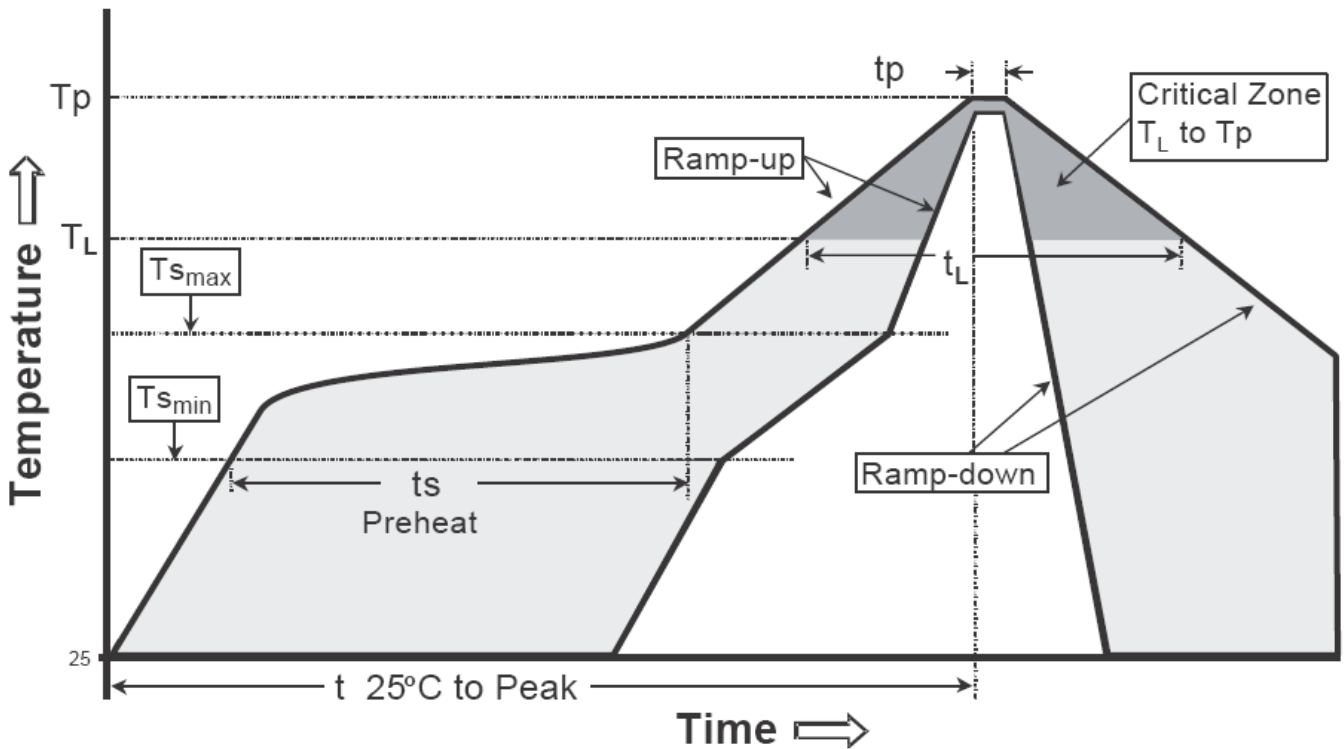
Safe Operating Area



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

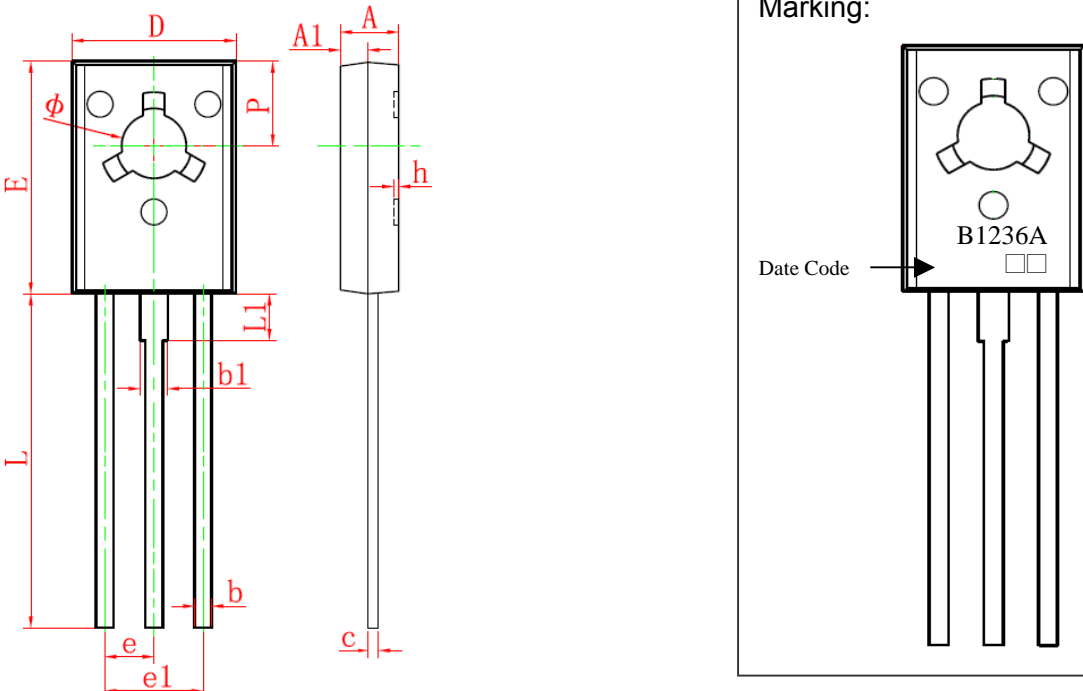
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _p)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(t _p)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-126 Dimension



Marking: **B1236A**
 Date Code

Style: Pin 1. Emitter 2. Collector 3. Base
 3-Lead TO-126 Plastic Package
 CYStek Package Code: T3

*: Typical

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	2.500	2.900	0.098	0.114	e	*2.290		*0.090	
A1	1.100	1.500	0.043	0.059	e1	4.480	4.680	0.176	0.184
b	0.660	0.860	0.026	0.034	h	0.000	0.300	0.000	0.012
b1	1.170	1.370	0.046	0.054	L	15.300	15.700	0.602	0.618
c	0.450	0.600	0.018	0.024	L1	2.100	2.300	0.083	0.091
D	7.400	7.800	0.291	0.307	P	3.900	4.100	0.154	0.161
E	10.600	11.000	0.417	0.433	Φ	3.000	3.200	0.118	0.126

- Notes: 1. Controlling dimension: millimeters.
 2. Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3. If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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