

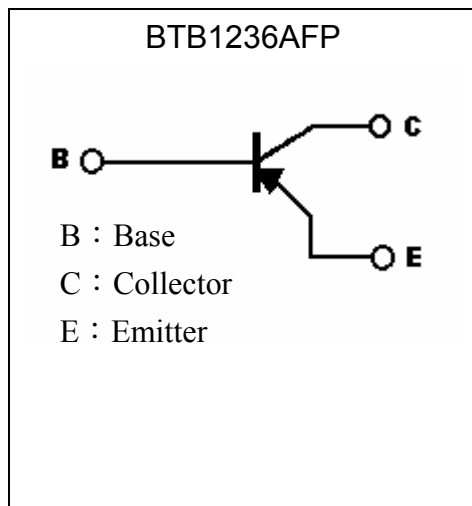
Silicon PNP Epitaxial Planar Transistor

BTB1236AFP

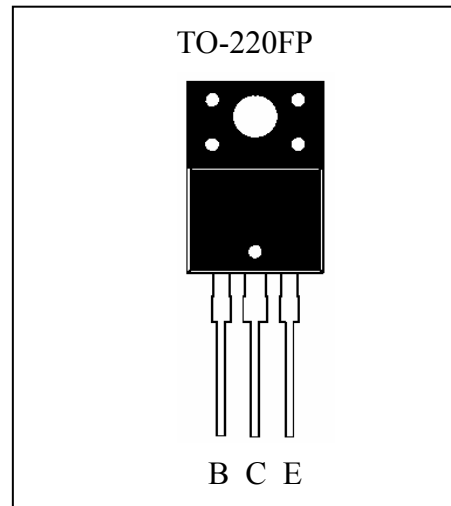
Description

- High BV_{CEO}
- High current capability
- RoHS compliant package

Symbol



Outline



Absolute Maximum Ratings (Ta=25°C)

Parameter		Symbol	Limits	Unit
Collector-Base Voltage		V_{CBO}	-180	V
Collector-Emitter Voltage		V_{CEO}	-160	
Emitter-Base Voltage		V_{EBO}	-5	
Collector Current (DC)		I_C	-1.5	A
Collector Current (Pulse)		I_{CP}	-3 (Note 1)	
Power Dissipation	T _A =25°C	P _D	2	W
	T _C =25°C		20	
Thermal Resistance, Junction to Ambient		R _{θJA}	62.5	°C/W
Thermal Resistance, Junction to Case		R _{θJC}	6.25	
Junction Temperature and Storage Temperature Range		T _j ; T _{stg}	-55~+150	°C

Note : 1. Single Pulse Pw ≤ 350μs, Duty ≤ 2%.

**Characteristics (Ta=25°C)**

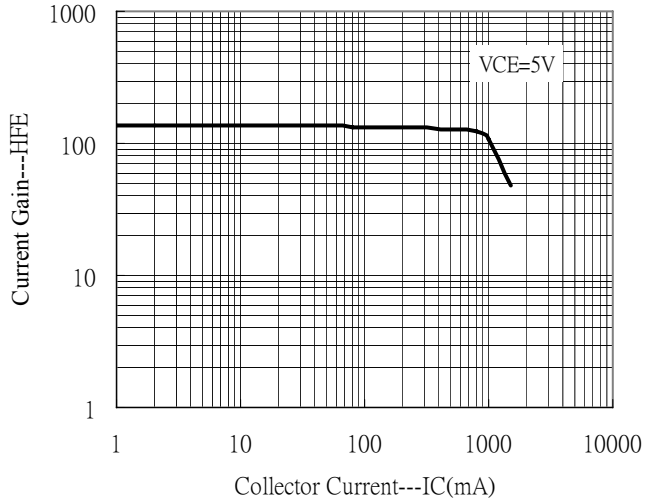
Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV_{CBO}	-180	-	-	V	$I_C=-50\mu A, I_E=0$
BV_{CEO}	-160	-	-	V	$I_C=-1mA, I_B=0$
BV_{EBO}	-5	-	-	V	$I_E=-50\mu A, I_C=0$
I_{CBO}	-	-	-1	μA	$V_{CB}=-160V, I_E=0$
I_{EBO}	-	-	-1	μA	$V_{EB}=-4V, I_C=0$
* $V_{CE(sat)}$	-	-	-0.12	V	$I_C=-250mA, I_B=-25mA$
* $V_{CE(sat)}$	-	-	-0.18	V	$I_C=-500mA, I_B=-50mA$
* $V_{CE(sat)}$	-	-0.24	-0.32	V	$I_C=-1A, I_B=-100mA$
* $R_{CE(sat)}$	-	-0.24	-0.32	Ω	$I_C=-1A, I_B=-100mA$
* $V_{BE(sat)}$	-	-	-1.1	V	$I_C=-1A, I_B=-100mA$
* $V_{BE(on)}$	-	-	-1	V	$V_{CE}=-5V, I_C=-150mA$
h_{FE1}	180	-	-	-	$V_{CE}=-5V, I_C=-1mA$
h_{FE2}	180	-	390	-	$V_{CE}=-5V, I_C=-100mA$
h_{FE3}	160	-	-	-	$V_{CE}=-5V, I_C=-500mA$
h_{FE4}	150	-	-	-	$V_{CE}=-5V, I_C=-1A$
f_T	-	180	-	MHz	$V_{CE}=-5V, I_C=-150mA$
Cob	-	24	-	pF	$V_{CB}=-10V, I_E=0, f=1MHz$

*Pulse Test: Pulse Width $\leq 380\mu s$, Duty Cycle $\leq 2\%$ **Ordering Information**

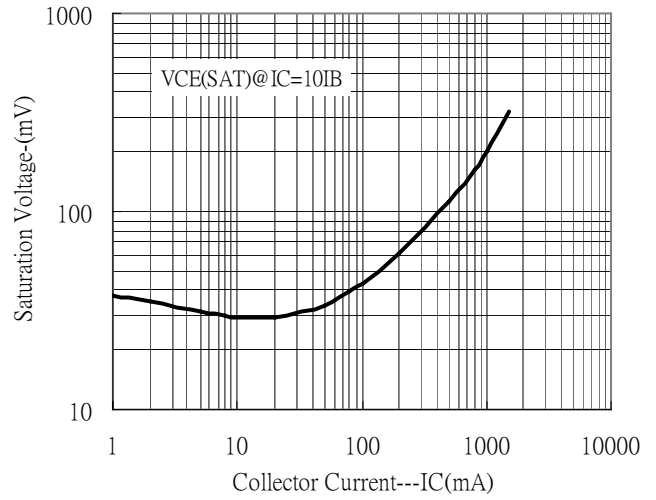
Device	Package	Shipping
BTB1236AFP	TO-220FP (Pb-free lead plating package)	50 pcs / tube, 40 tubes / boxes

Characteristic Curves

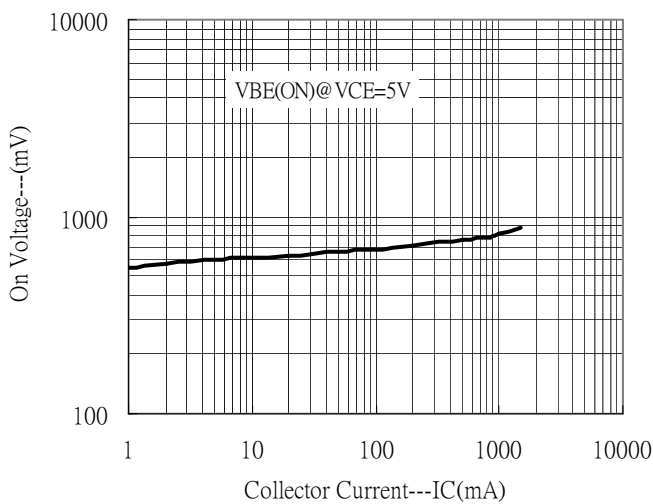
Current Gain vs Collector Current



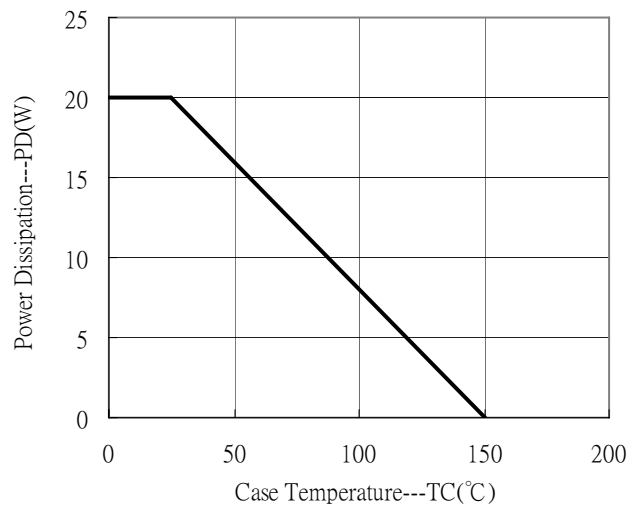
Saturation Voltage vs Collector Current



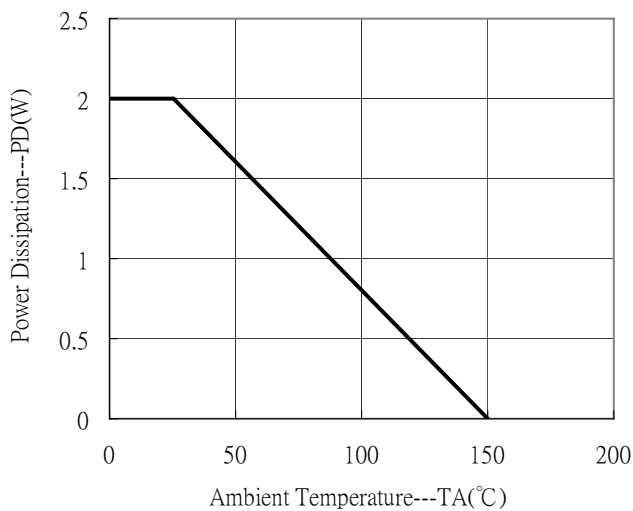
On Voltage vs Collector Current



Power Derating Curve



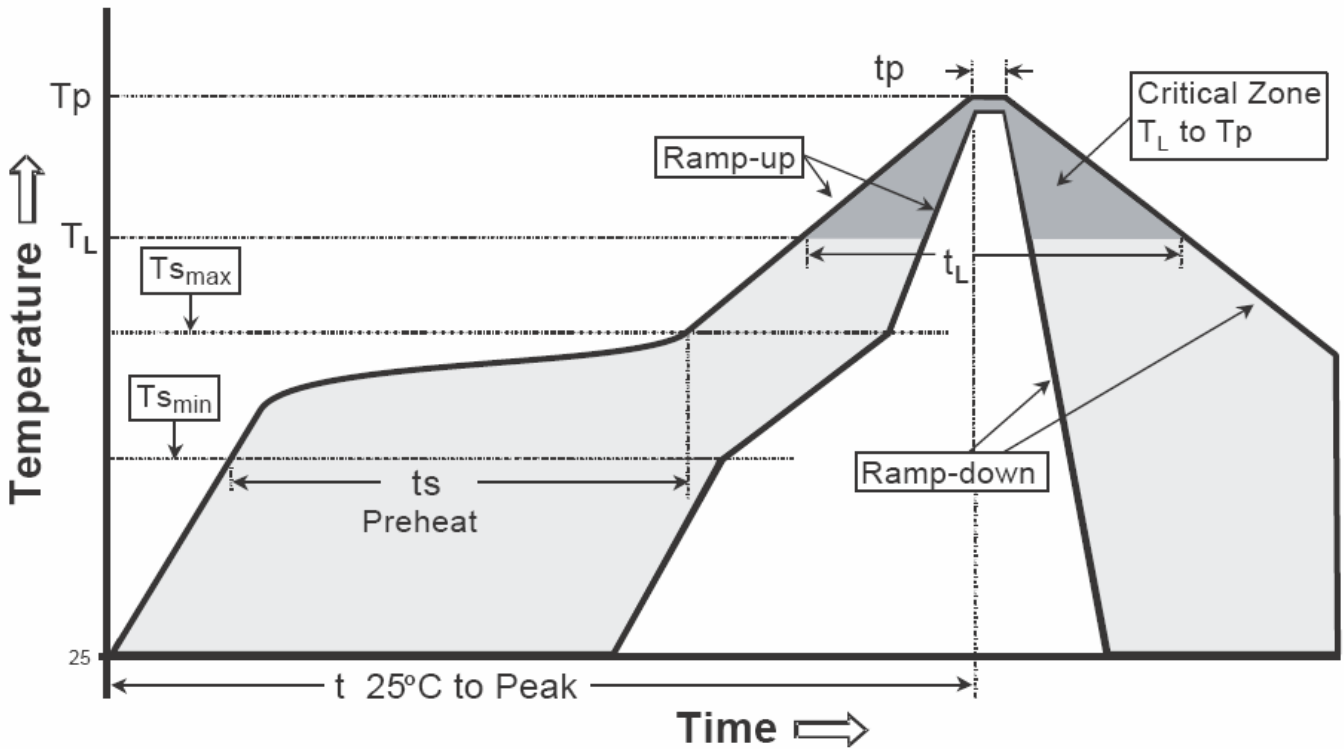
Power Derating Curve



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

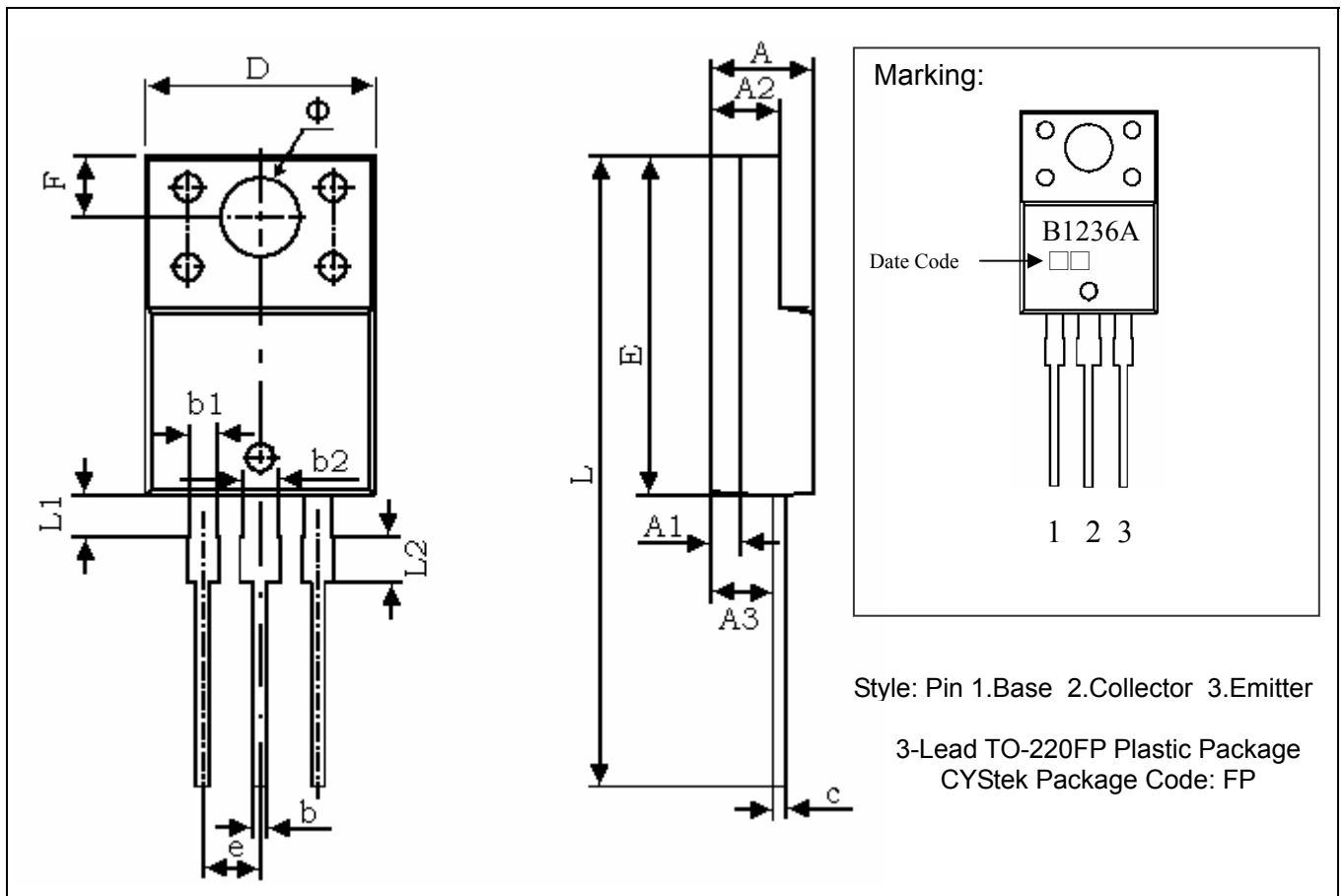
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _P)	220 +0/-5 °C	245 +0/-5 °C
Time within 5°C of actual peak temperature(t _p)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-220FP Dimension



*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.169	0.185	4.300	4.700	D	0.392	0.408	9.960	10.360
A1	0.051 REF		1.300 REF		E	0.583	0.598	14.800	15.200
A2	0.110	0.126	2.800	3.200	e	0.100 TYP		2.540 TYP	
A3	0.098	0.114	2.500	2.900	F	0.106 REF		2.700 REF	
b	0.020	0.030	0.500	0.750	Φ	0.138 REF		3.500 REF	
b1	0.043	0.053	1.100	1.350	L	1.102	1.118	28.000	28.400
b2	0.059	0.069	1.500	1.750	L1	0.067	0.075	1.700	1.900
c	0.020	0.030	0.500	0.750	L2	0.075	0.083	1.900	2.100

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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