

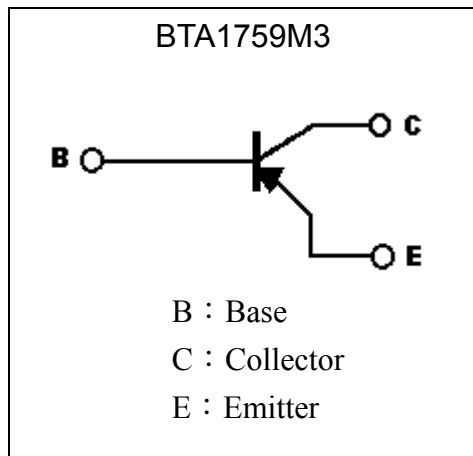
High Voltage PNP Epitaxial Planar Transistor

BTA1759M3

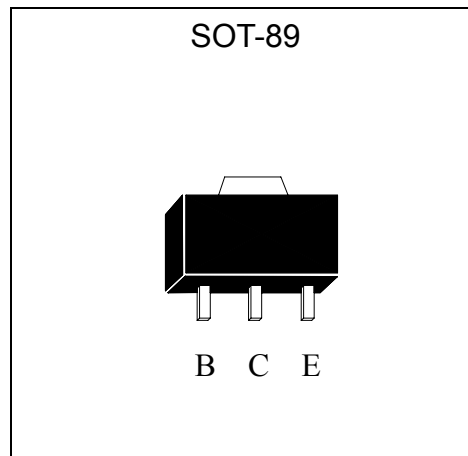
Description

- High breakdown voltage. ($BV_{CEO} = -400V$)
- Low saturation voltage, typically $V_{CE(sat)} = -0.12V$ at $I_C/I_B = -10mA/-1mA$.
- Wide SOA (safe operation area).
- Complementary to BTC4505M3.
- Pb-free lead plating and halogen-free package
- Weight : approx. 48.34 mg

Symbol

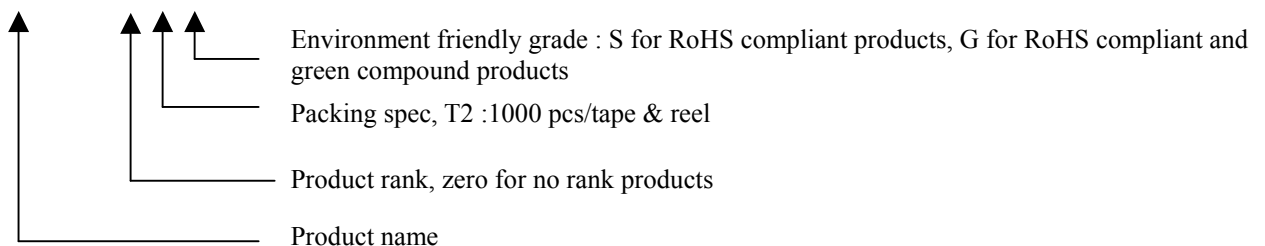


Outline



Ordering Information

Device	Package	Shipping
BTA1759M3-Q-T2-G	SOT-89 (Pb-free lead plating and halogen-free package)	1000 pcs / Tape & Reel





Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V _{CB0}	-400	V
Collector-Emitter Voltage	V _{CEO}	-400	V
Emitter-Base Voltage	V _{EBO}	-6	V
Collector Current	I _C	-300	mA
Power Dissipation	P _D	0.6	W
		1 (Note 1)	W
		2 (Note 2)	W
Thermal Resistance, Junction to Ambient	R _{θJA}	208	°C/W
		125 (Note 1)	°C/W
		62.5 (Note 2)	°C/W
Junction Temperature	T _j	150	°C
Storage Temperature	T _{stg}	-55~+150	°C

Note : 1. When mounted on FR-4 PCB with area measuring 10×10×1 mm
 2. When mounted on ceramic with area measuring 40×40×1 mm

Characteristics (Ta=25°C)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV _{CB0}	-400	-	-	V	I _C =-50μA
BV _{CEO}	-400	-	-	V	I _C =-1mA
BV _{EBO}	-6	-	-	V	I _E =-50μA
IC _{B0}	-	-	-100	nA	V _{CB} =-400V
I _{EBO}	-	-	-100	nA	V _{EB} =-6V
ICES	-	-	-500	nA	V _{CB} =-400V
V _{CE(sat)} 1	-	-	-0.2	V	I _C =-1mA, I _B =-0.1mA
*V _{CE(sat)} 2	-	-	-0.3	V	I _C =-10mA, I _B =-1mA
*V _{CE(sat)} 3	-	-	-0.6	V	I _C =-50mA, I _B =-5mA
*V _{BE(sat)}	-	-	-0.9	V	I _C =-20mA, I _B =-2mA
h _{FE} 1	60	-	-	-	V _{CE} =-10V, I _C =-1mA
*h _{FE} 2	120	-	270	-	V _{CE} =-10V, I _C =-10mA
*h _{FE} 3	50	-	-	-	V _{CE} =-10V, I _C =-50mA
*h _{FE} 4	40	-	-	-	V _{CE} =-10V, I _C =-100mA
C _{ob}	-	-	6	pF	V _{CB} =-10V, I _E =0A, f=1MHz

*Pulse Test: Pulse Width ≤380μs, Duty Cycle ≤2%

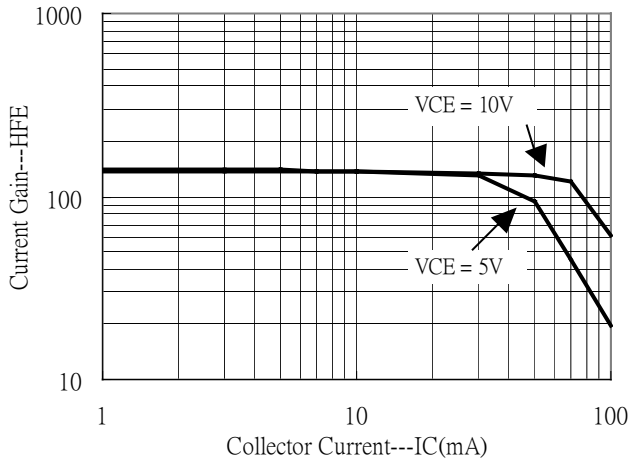
Classification Of h_{FE}

Rank	Q
Range	120~270

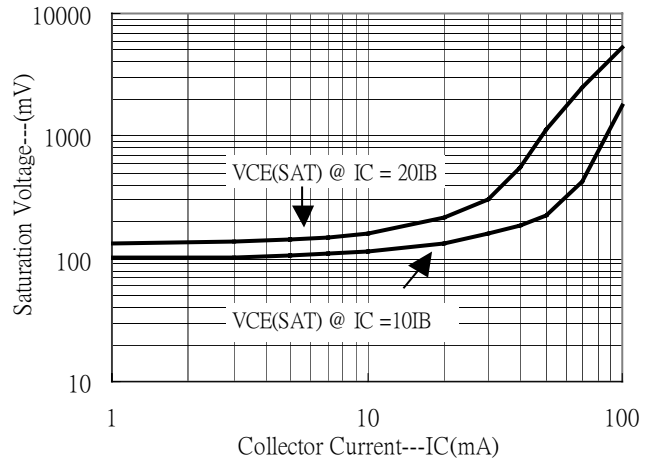


Typical Characteristics

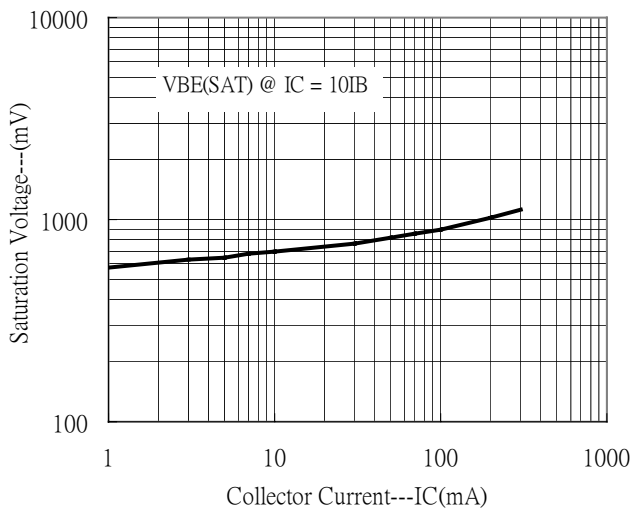
Current Gain vs Collector Current



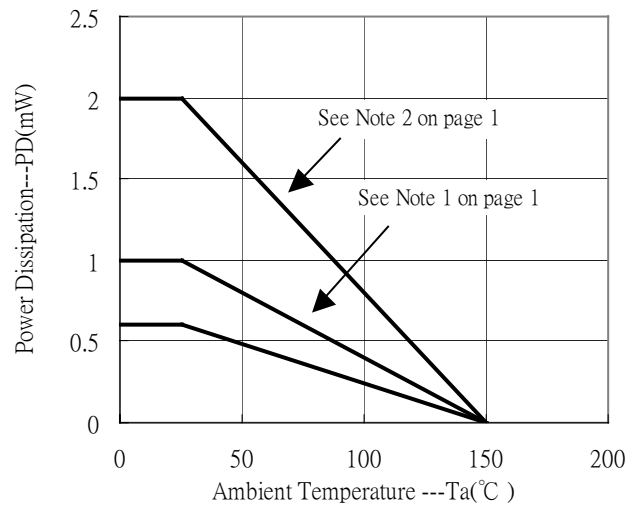
Saturation Voltage vs Collector Current



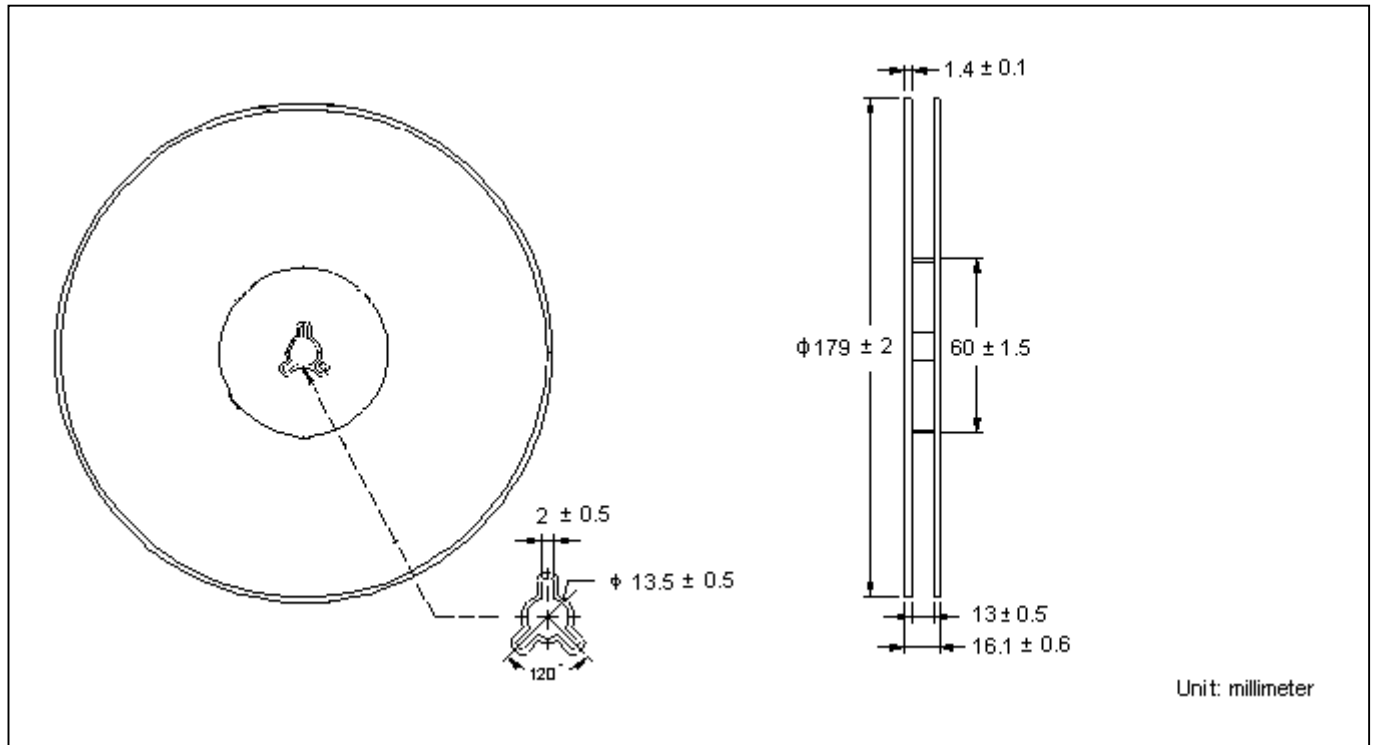
Saturation Voltage vs Collector Current



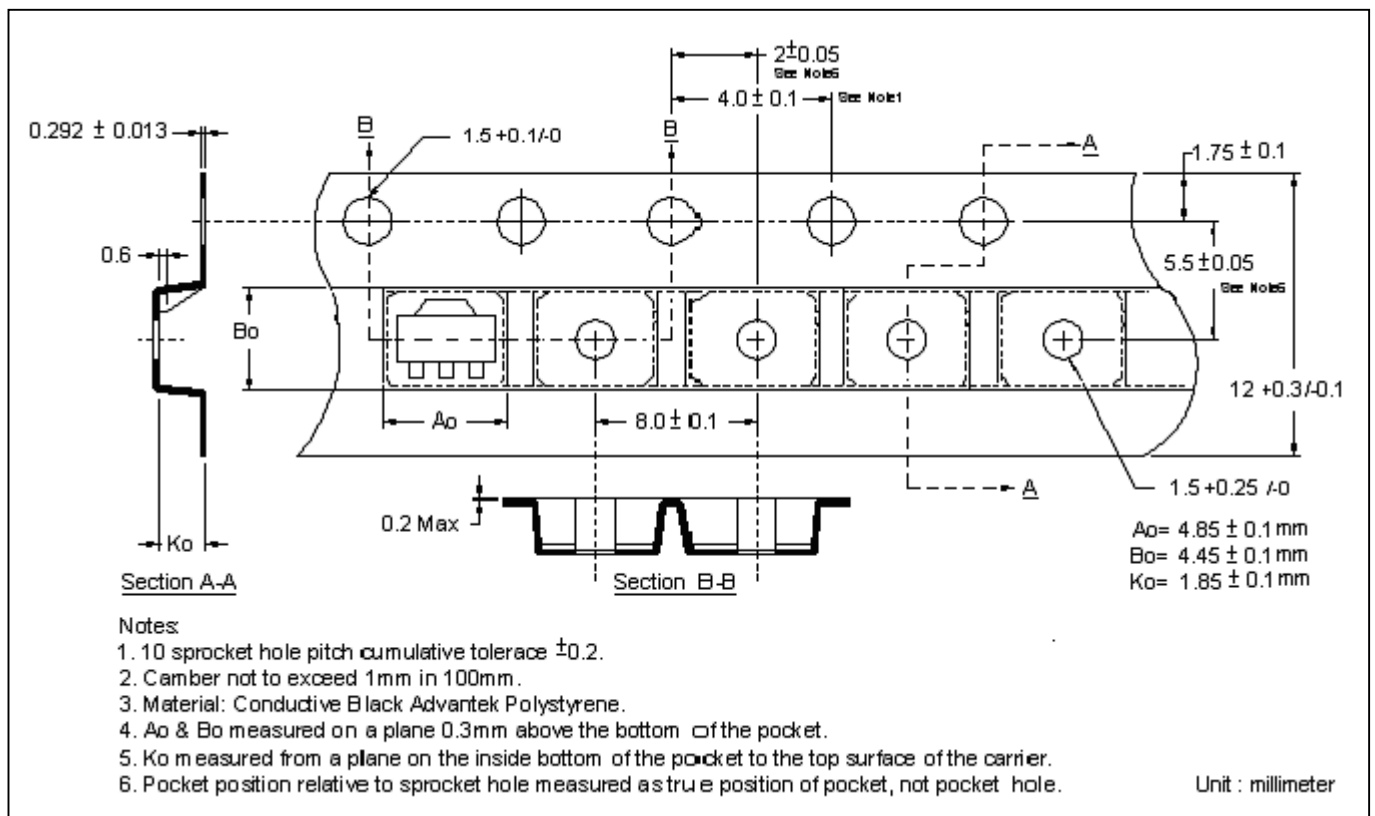
Power Derating Curves



Reel Dimension



Carrier Tape Dimension



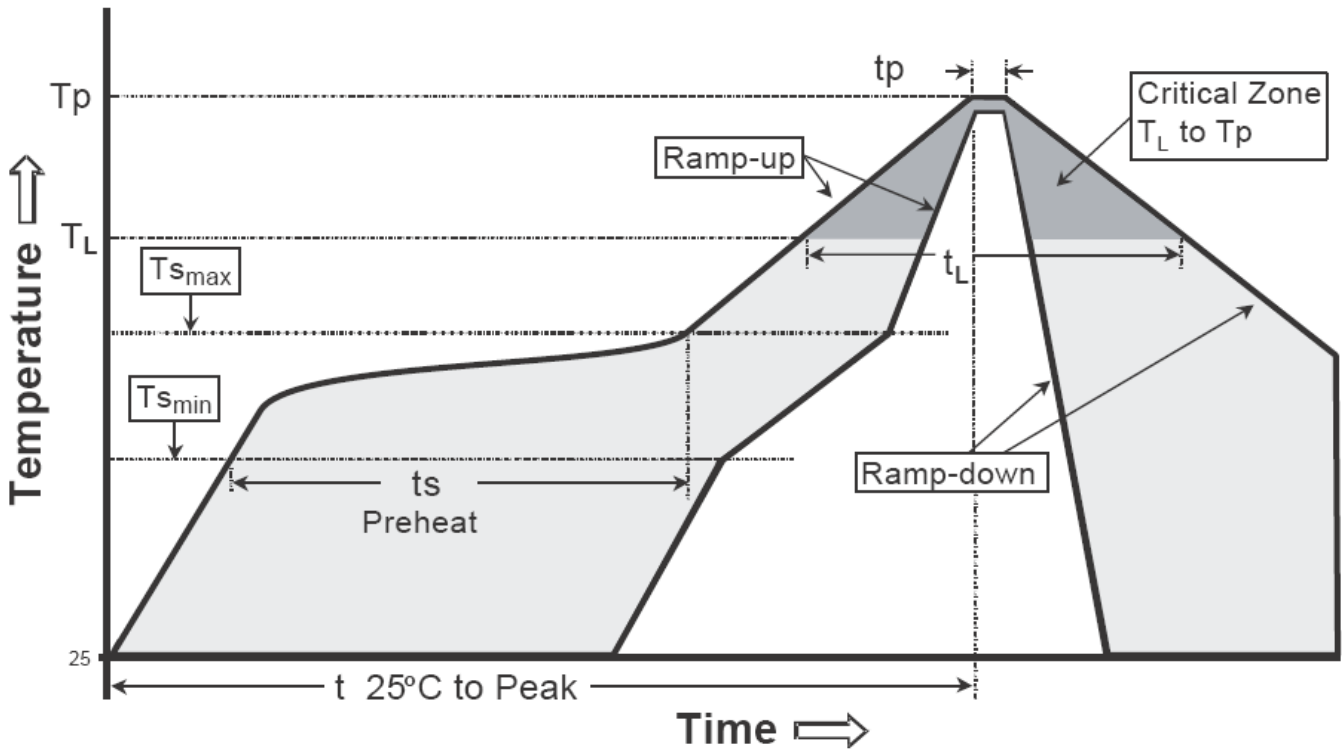
Notes

1. 10 sprocket hole pitch cumulative tolerance ± 0.2 .
2. Camber not to exceed 1mm in 100mm.
3. Material: Conductive Black Advantek Polystyrene.
4. A_o & B_o measured on a plane 0.3mm above the bottom of the pocket.
5. K_o measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

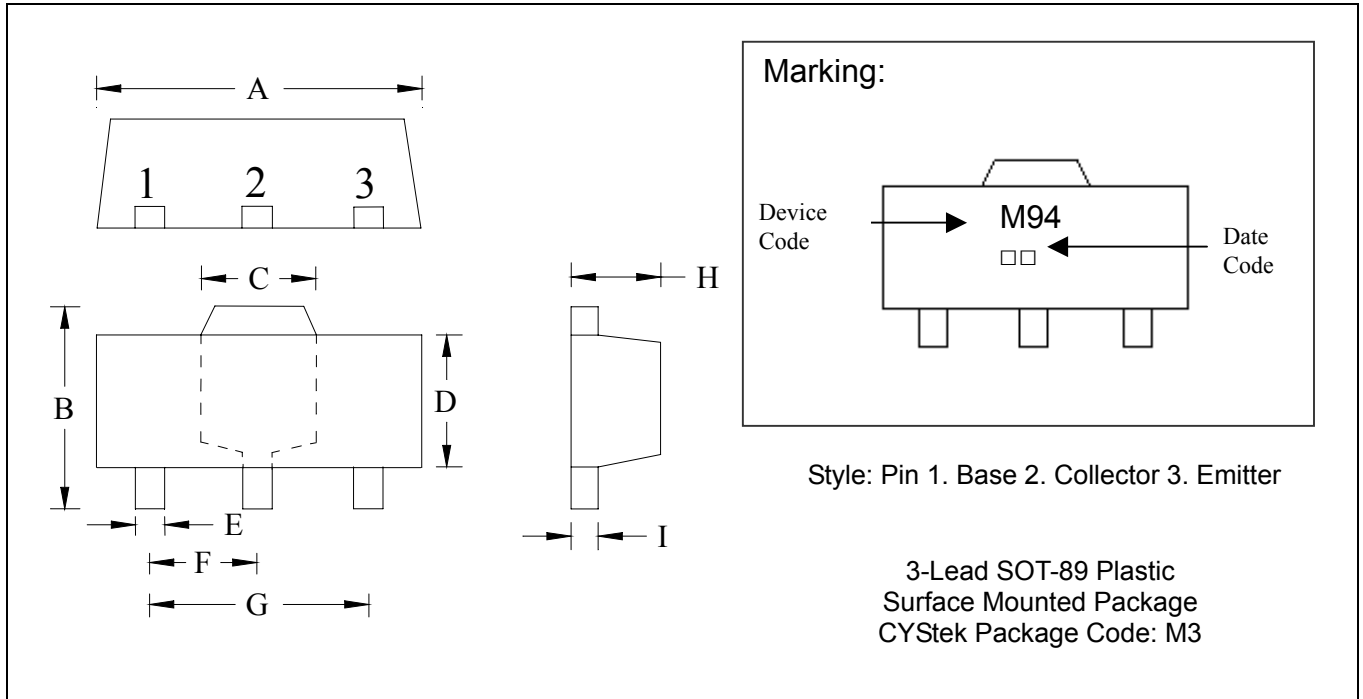
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note :1. All temperatures refer to topside of the package, measured on the package body surface.
 2.For devices mounted on FR-4 PCB of 1.6mm or equivalent grade PCB. If other grade PCB is used, care should be taken to match the coefficients of thermal expansion between components and PCB. If they are not matched well, the solder joints may crack or the bodies of the parts may crack or shatter as the assembly cools.

SOT-89 Dimension



*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1732	0.1811	4.40	4.60	F	0.0583	0.0598	1.48	1.527
B	0.1594	0.1673	4.05	4.25	G	0.1165	0.1197	2.96	3.04
C	0.0591	0.0663	1.50	1.70	H	0.0551	0.0630	1.40	1.60
D	0.0945	0.1024	2.40	2.60	I	0.0138	0.0161	0.35	0.41
E	0.01417	0.0201	0.36	0.51					

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0

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