

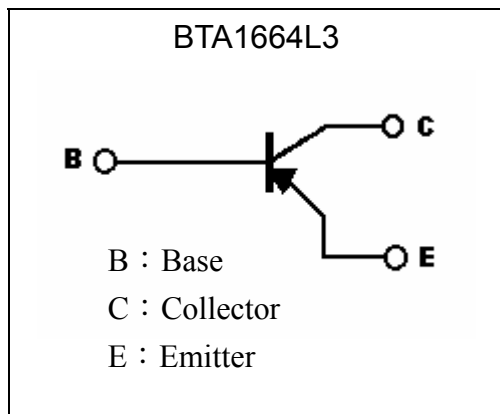
Low Vcesat PNP Epitaxial Planar Transistor

BTA1664L3

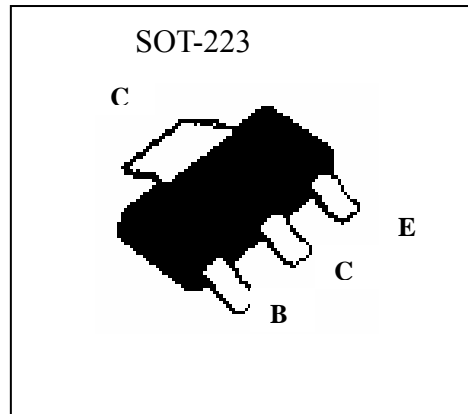
Features

- Low VCE(sat), VCE(sat)=-0.24V (typical), at IC / IB =- 500mA /- 20mA
- Pb-free lead plating and halogen-free package

Symbol



Outline



Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V _{CBO}	-40	V
Collector-Emitter Voltage	V _{CEO}	-25	V
Emitter-Base Voltage	V _{EBO}	-5	V
Collector Current(DC)	I _C	-2	A
Peak Collector Current	I _{CM}	-4	A
Peak Base Current	I _{BM}	-200	mA
Power Dissipation @T _A =25°C	P _d	3 (Note)	W
Junction Temperature	T _j	150	°C
Storage Temperature	T _{stg}	-55~+150	°C

Note : The power which can be dissipated assuming the device is mounted in a typical manner on a P.C.B. with copper equal to 4 square inch minimum.

**Characteristics (Ta=25°C)**

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV _{CB0}	-40	-	-	V	I _C =-50μA, I _E =0
BV _{CE0}	-25	-	-	V	I _C =-1mA, I _B =0
BV _{EB0}	-5	-	-	V	I _E =-50μA, I _C =0
I _{CB0}	-	-	-100	nA	V _{CB} =-40V, I _E =0
I _{EB0}	-	-	-100	nA	V _{EB} =-5V, I _C =0
*V _{CE(sat)}	-	-0.24	-0.4	V	I _C =-500mA, I _B =-20mA
*V _{BE(on)}	-0.5	-	-0.8	V	V _{CE} =-1V, I _C =-10mA
*h _{FE 1}	120	-	390	-	V _{CE} =-1V, I _C =-100mA
*h _{FE 2}	40	-	-	-	V _{CE} =-1V, I _C =-700mA
f _T	-	120	-	MHz	V _{CE} =-5V, I _C =-10mA, f=100MHz
Cob	-	19	-	pF	V _{CB} =-10V, f=1MHz

*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

Classification of h_{FE 1}

Rank	Q	R
Range	120~270	180~390

Ordering Information

Device	Package	Shipping	Marking
BTA1664L3	SOT-223 (Pb-free lead plating and halogen-free package)	2500 pcs / Tape & Reel	A1664

Moisture Sensitivity Level : Conform to JEDEC Level 3

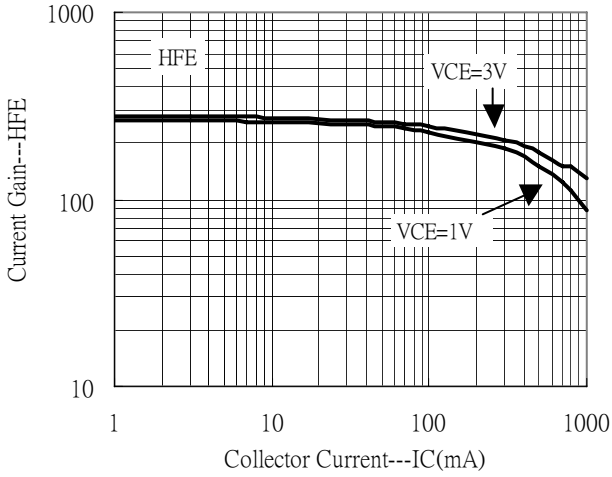
Recommended Storage Condition:

Temperature : ≤ 30 °C

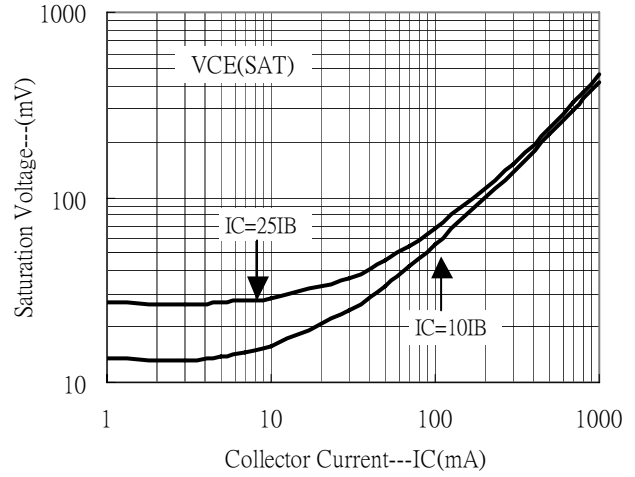
Humidity : ≤ 60% RH

Characteristic Curves

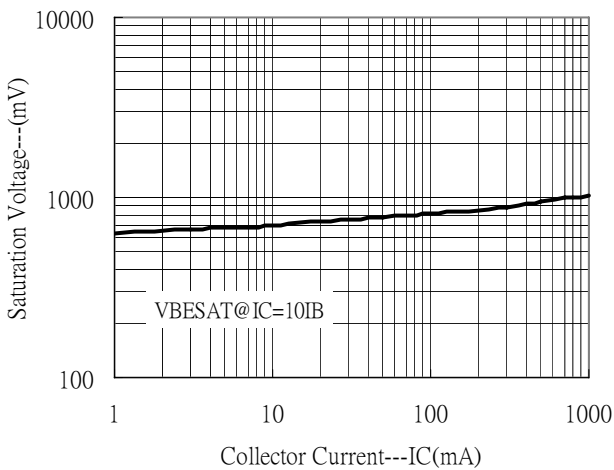
Current Gain vs Collector Current



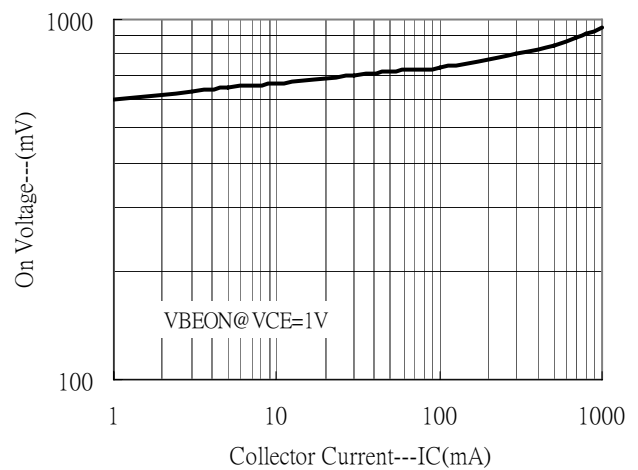
Saturation Voltage vs Collector Current



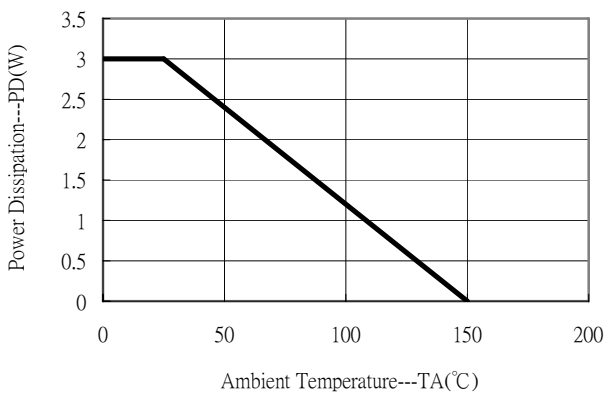
Saturation Voltage vs Collector Current



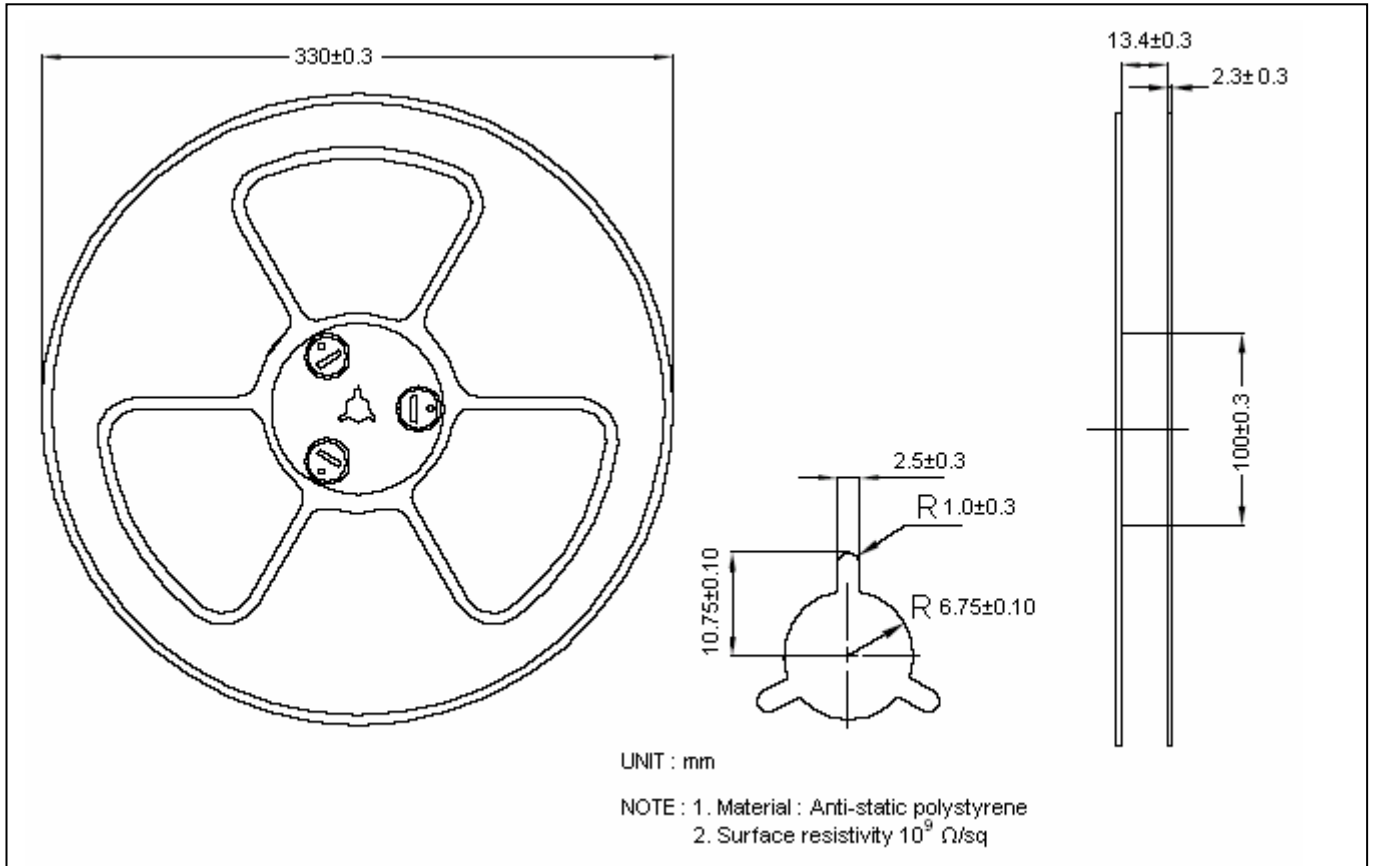
On Voltage vs Collector Current



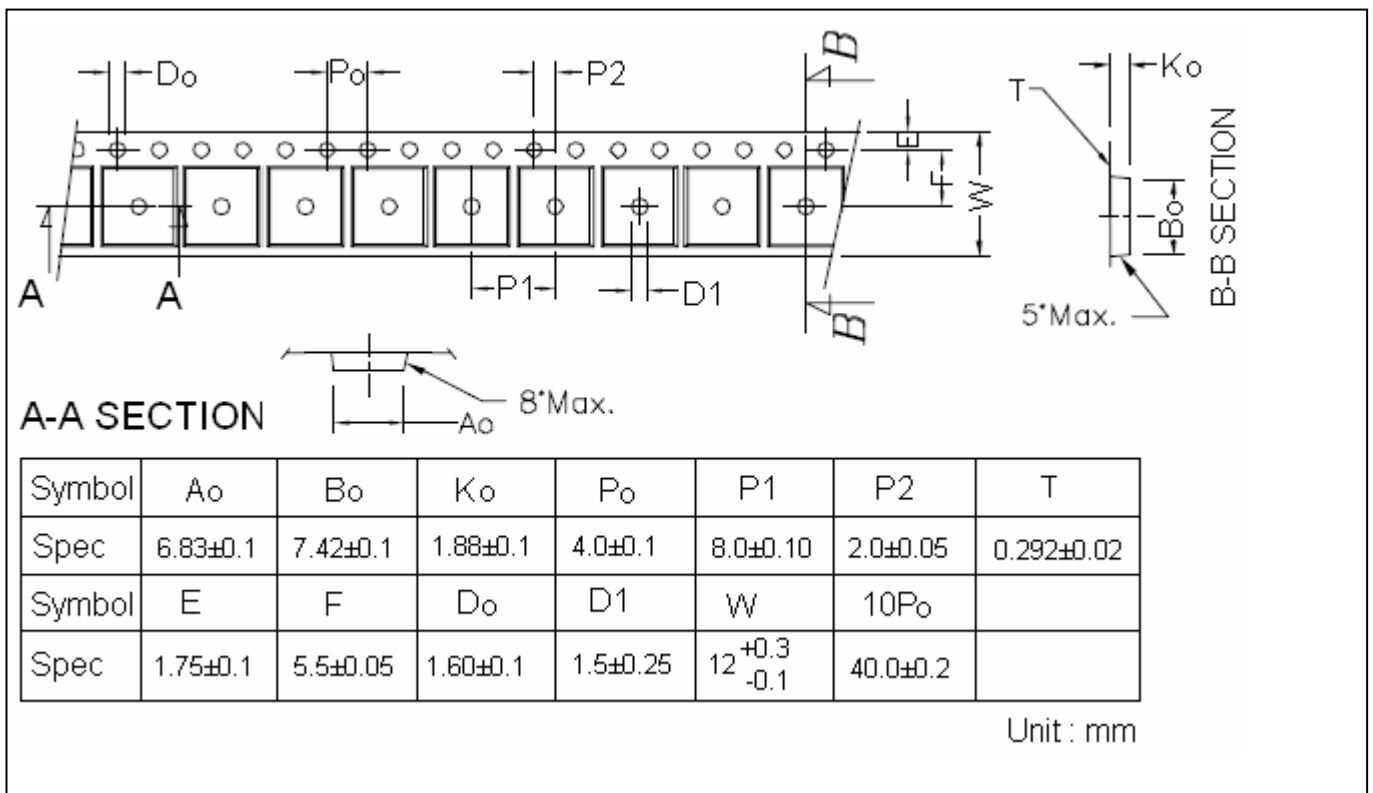
Power Derating Curve



Reel Dimension



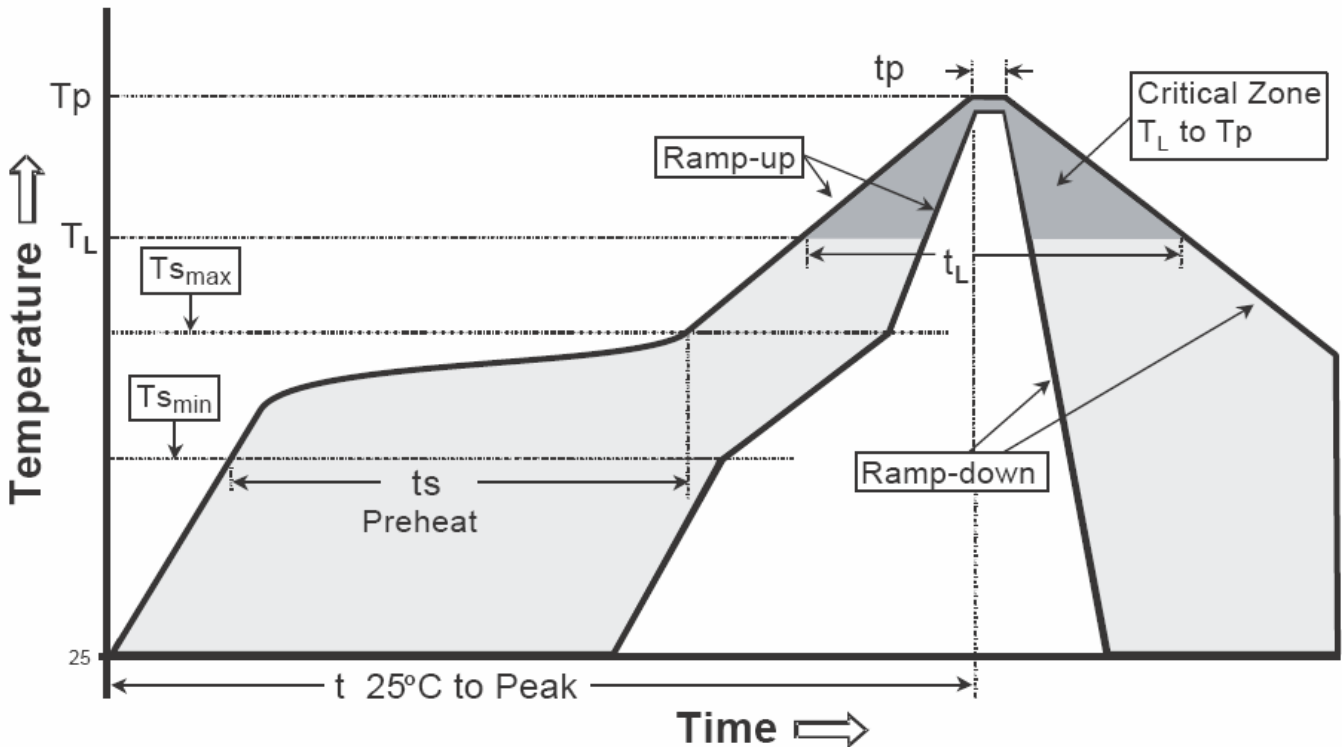
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

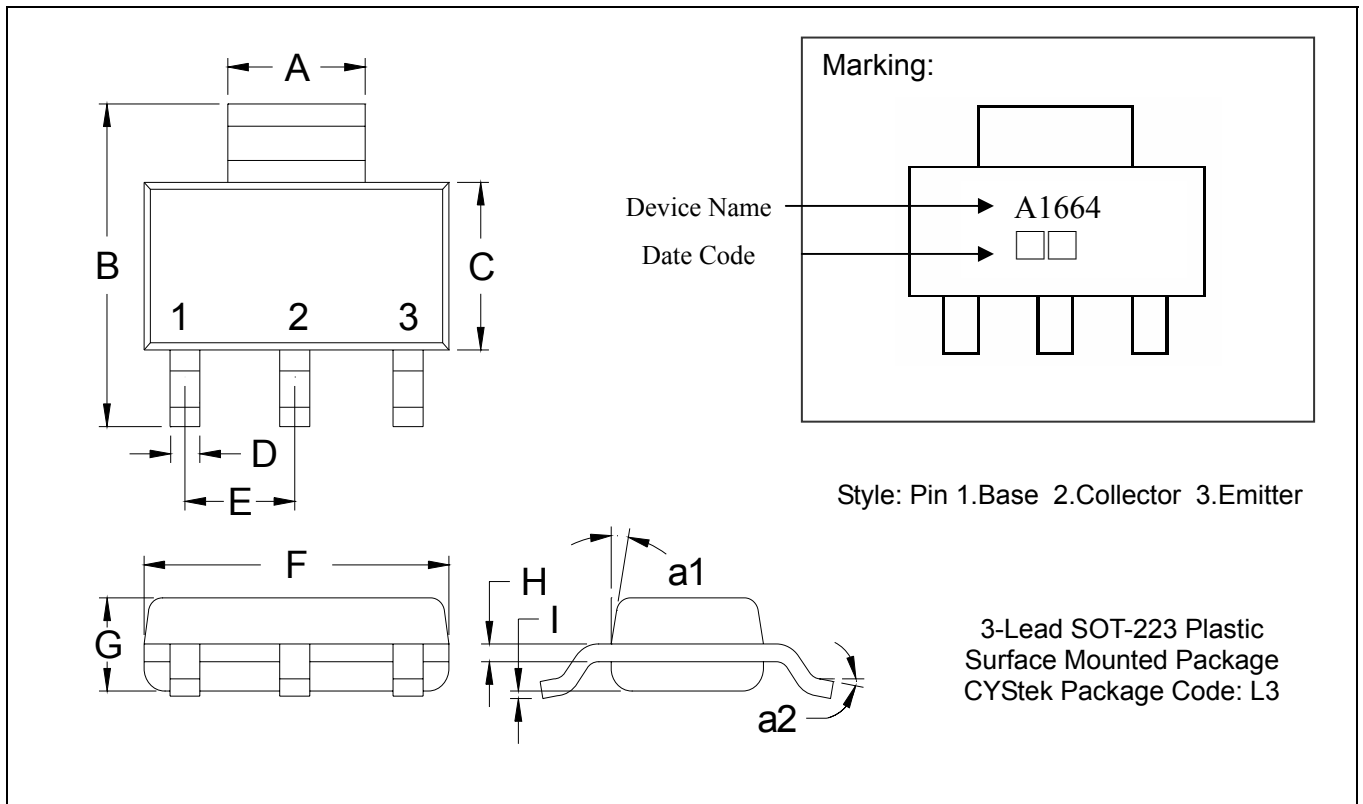
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

SOT-223 Dimension



*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1142	0.1220	2.90	3.10	G	0.0551	0.0709	1.40	1.80
B	0.2638	0.2874	6.70	7.30	H	0.0098	0.0138	0.25	0.35
C	0.1299	0.1457	3.30	3.70	I	0.0008	0.0039	0.02	0.10
D	0.0236	0.0315	0.60	0.80	a1	*13°	-	*13°	-
E	*0.0906	-	*2.30	-	a2	0°	10°	0°	10°
F	0.2480	0.2638	6.30	6.70					

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.