ESD protected N-Channel Enhancement Mode MOSFET

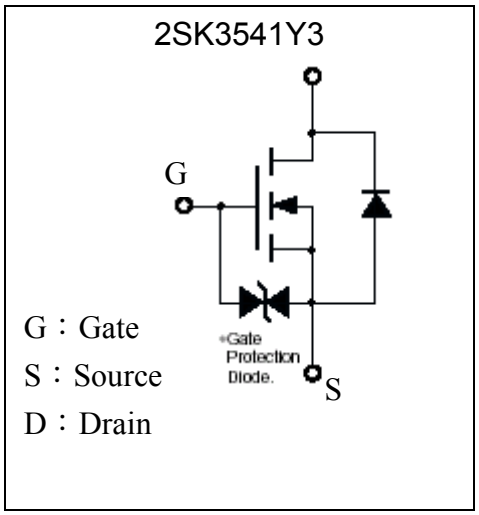
2SK3541Y3

BV_{DSS}	30V
I_D	100mA
R_{DSON}@4V	3.4Ω (TYP)
R_{DSON}@2.5V	6.9Ω (TYP)

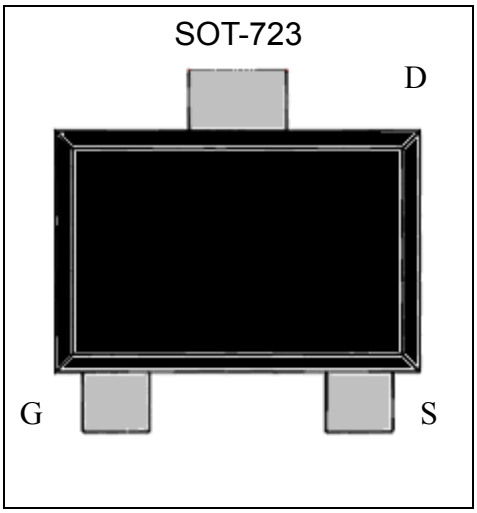
Description

- Low voltage drive(2.5V drive) makes this device ideal for portable equipment.
- High speed switching
- ESD protected device
- Pb-free lead plating & halogen-free package

Symbol



Outline



Ordering Information

Device	Package	Shipping
2SK3541Y3-0-T5-G	SOT-723 (Pb-free lead plating and halogen-free package)	8000 pcs / Tape & Reel

Environment friendly grade : S for RoHS compliant products, G for RoHS compliant and green compound products

Packing spec, T5 : 8000 pcs / tape & reel,7” reel

Product rank, zero for no rank products

Product name

Absolute Maximum Ratings (Ta=25°C)

Parameter		Symbol	Limits	Unit
Drain-Source Voltage		BV_{DSS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Drain Current	Continuous	I_D	±100	mA
	Pulsed	I_{DP}	±200 *1	mA
Reverse Drain Current	Continuous	I_{DR}	±100	mA
	Pulsed	I_{DRP}	±200 *1	mA
Total Power Dissipation		P_D	150 *2	mW
ESD susceptibility			750 *3	V
Operating Junction and Storage Temperature Range		Tj ; Tstg	-55~+150	°C
Thermal Resistance, Junction-to-Ambient		Rth,ja	833	°C/W

Note : *1. Pulse Width ≤ 10μs, Duty cycle ≤1%
*2. With each pin mounted on the recommended lands.
*3. Human body model, 1.5kΩ in series with 100pF

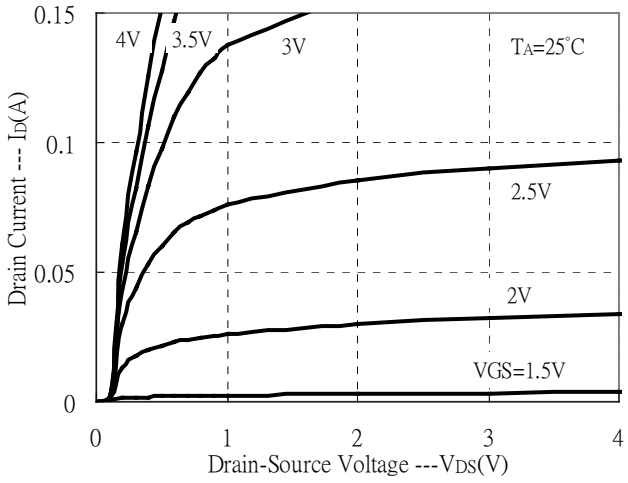
Electrical Characteristics (Ta=25°C)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV_{DSS}	30	-	-	V	V_{GS}=0, I_D=100μA
$V_{GS(th)}$	0.8	1.3	1.5	V	V_{DS}=3V, I_D=100μA
I_{GSS}	-	-	±1	μA	V_{GS}=±20V, V_{DS}=0
I_{DSS}	-	-	100	nA	V_{DS}=30V, V_{GS}=0
$R_{DS(ON)}$	-	3.4	8	Ω	V_{GS}=4V, I_D=10mA
	-	6.9	13		V_{GS}=2.5V, I_D=1mA
G_{FS}	20	50	-	mS	V_{DS}=3V, I_D=10mA
Dynamic					
C_{iss}	-	12.5	-	pF	V_{DS}=5V, V_{GS}=0, f=1MHz
C_{oss}	-	7.3	-		
C_{rss}	-	3.5	-		
$t_{d(on)}$	-	15	-	ns	V_{DD}≒5V, I_D=10mA, V_{GS}=5V, R_L=500Ω, R_G=10Ω
t_r	-	35	-		
$t_{d(off)}$	-	75	-		
t_f	-	75	-		
Source-Drain Diode					
*V_{SD}	-	0.88	1.2	V	V_{GS}=0V, I_S=100mA

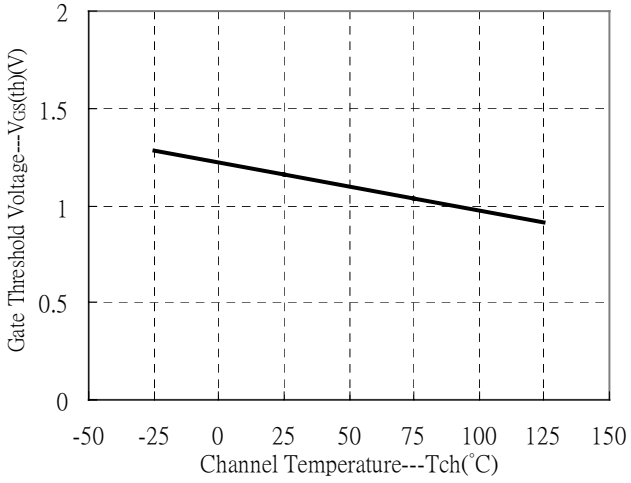
*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

Typical Characteristics

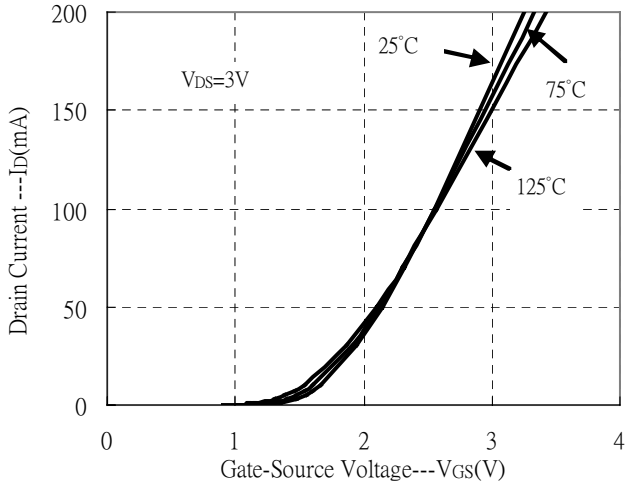
Typical Output Characteristics



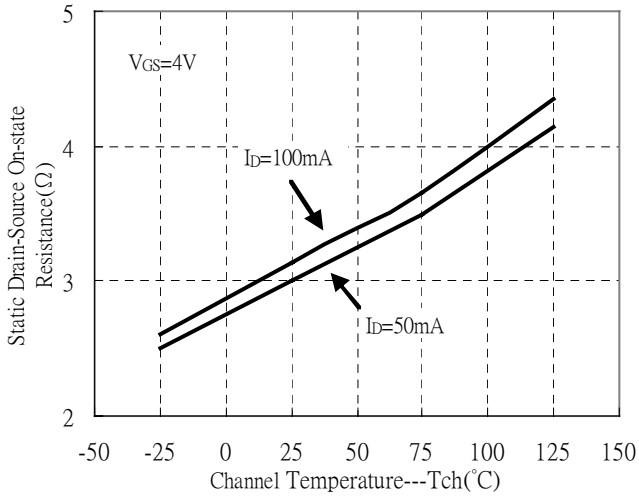
Gate Threshold Voltage vs Channel Temperature



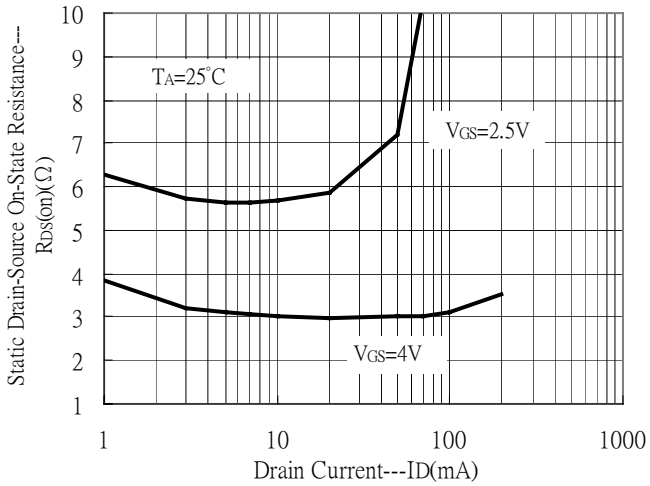
Typical Transfer Characteristics



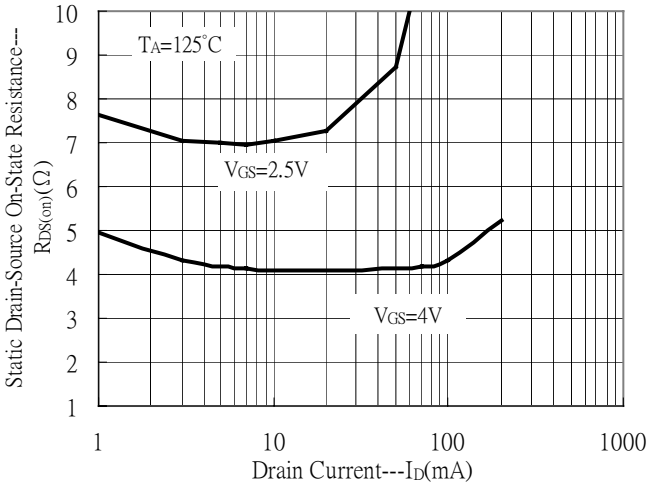
Static Drain-Source On-state Resistance with Temperature



Static Drain-Source On-State resistance vs Drain Current

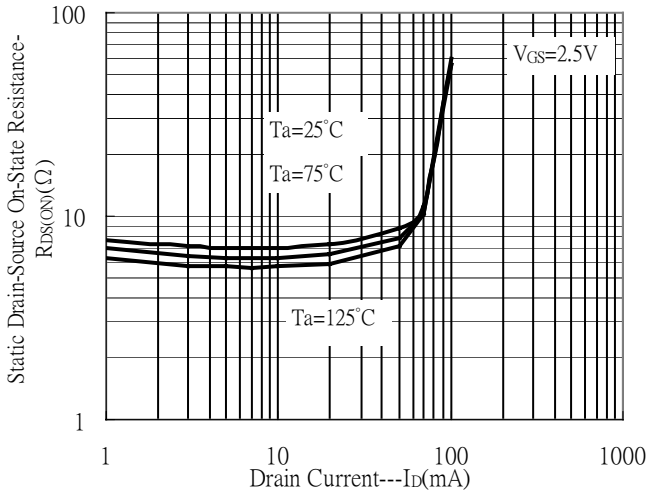


Static Drain-Source On-State resistance vs Drain Current

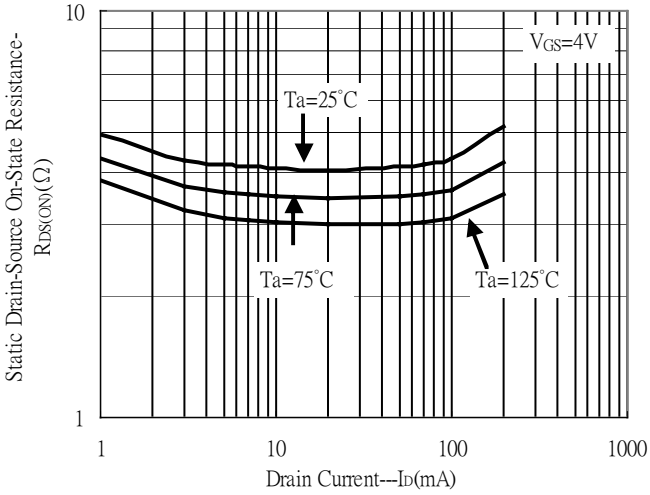


Typical Characteristics(Cont.)

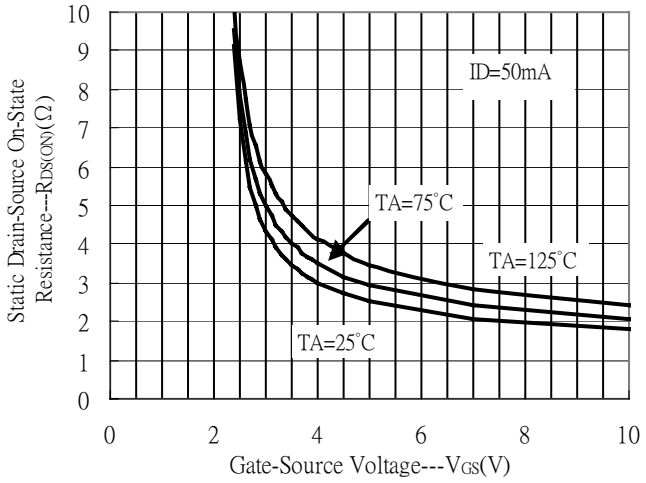
Static Drain-Source On-State Resistance vs Drain Current



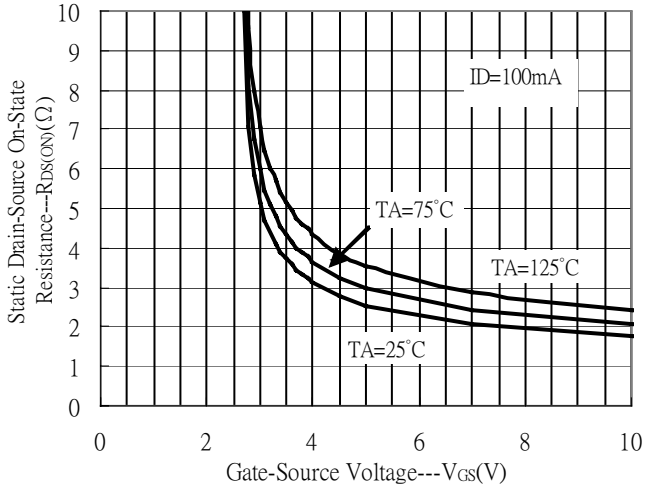
Static Drain-Source On-State Resistance vs Drain Current



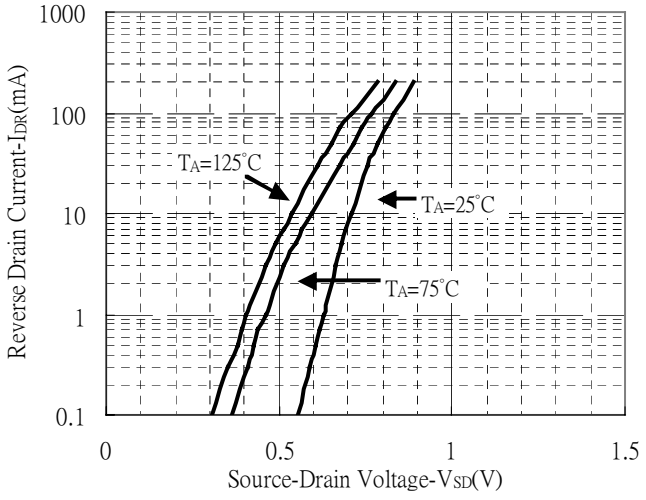
Static Drain-Source On-State Resistance vs Gate-Source Voltage



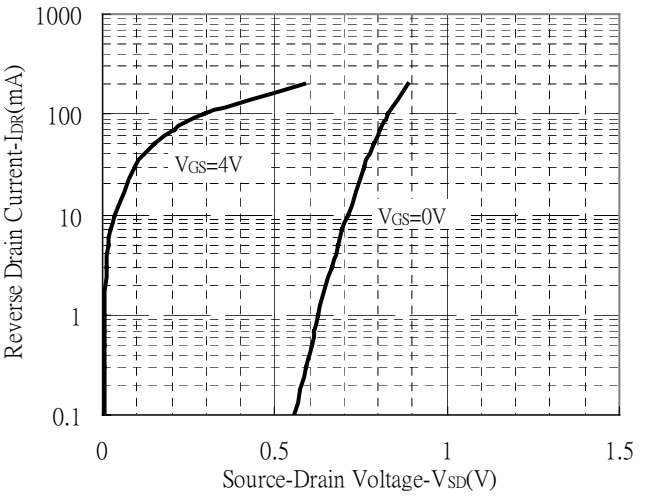
Static Drain-Source On-State Resistance vs Gate-Source Voltage



Reverse Drain Current vs Source-Drain Voltage(I)

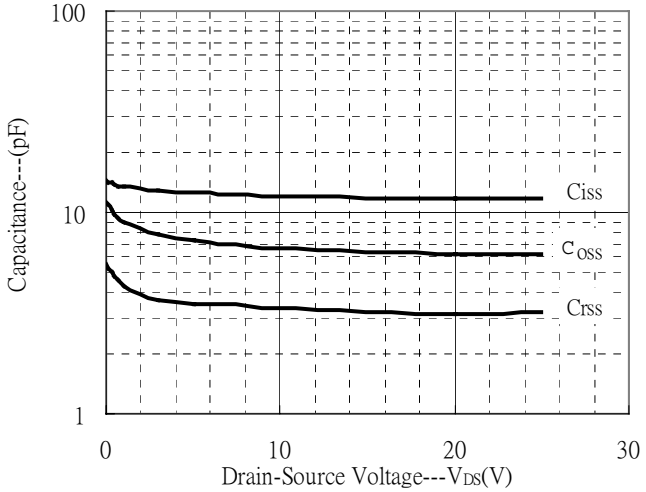


Reverse Drain Current vs Source-Drain Voltage(II)

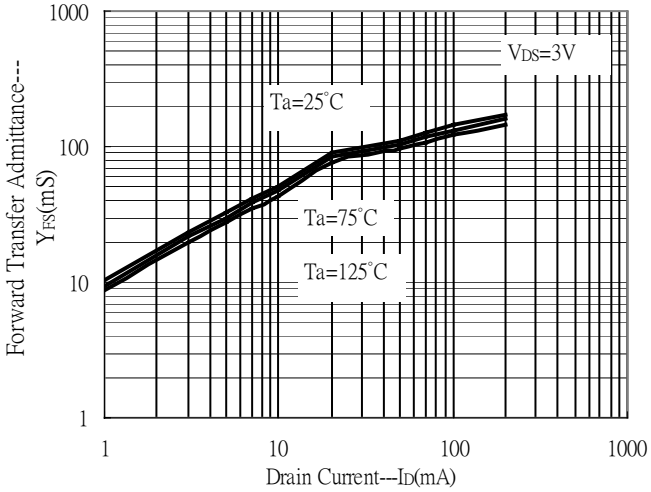


Typical Characteristics(Cont.)

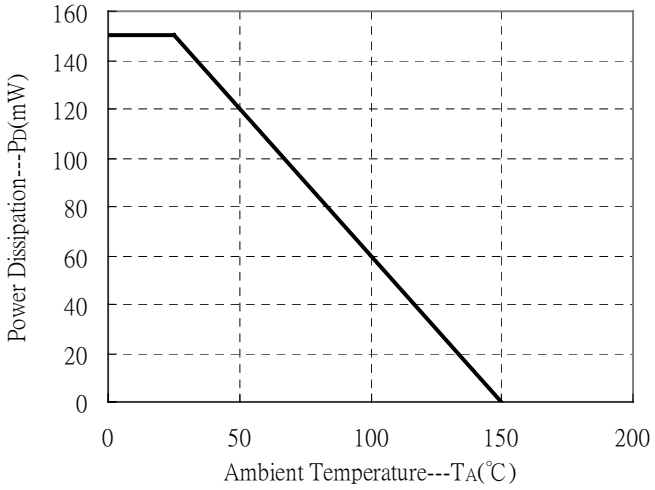
Capacitance vs Drain-to-Source Voltage



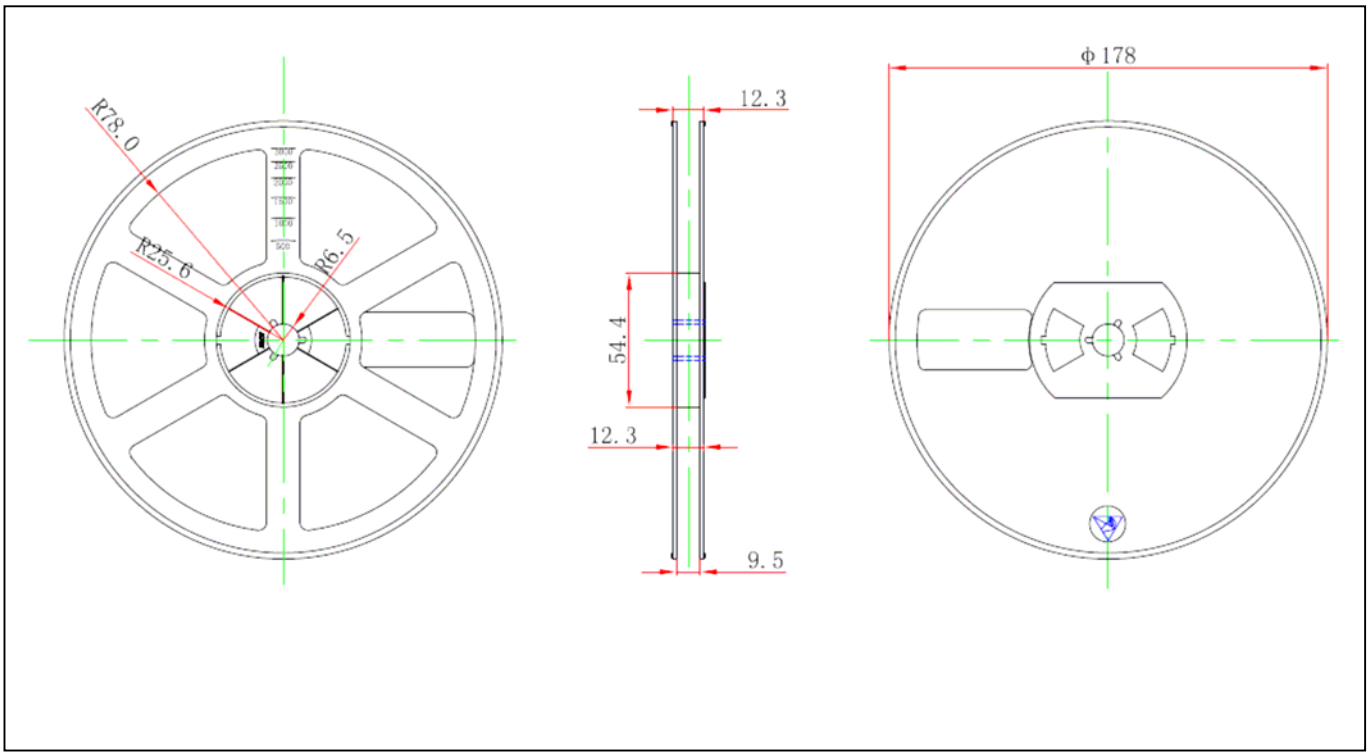
Foreward Transfer Admittance vs Drain Current



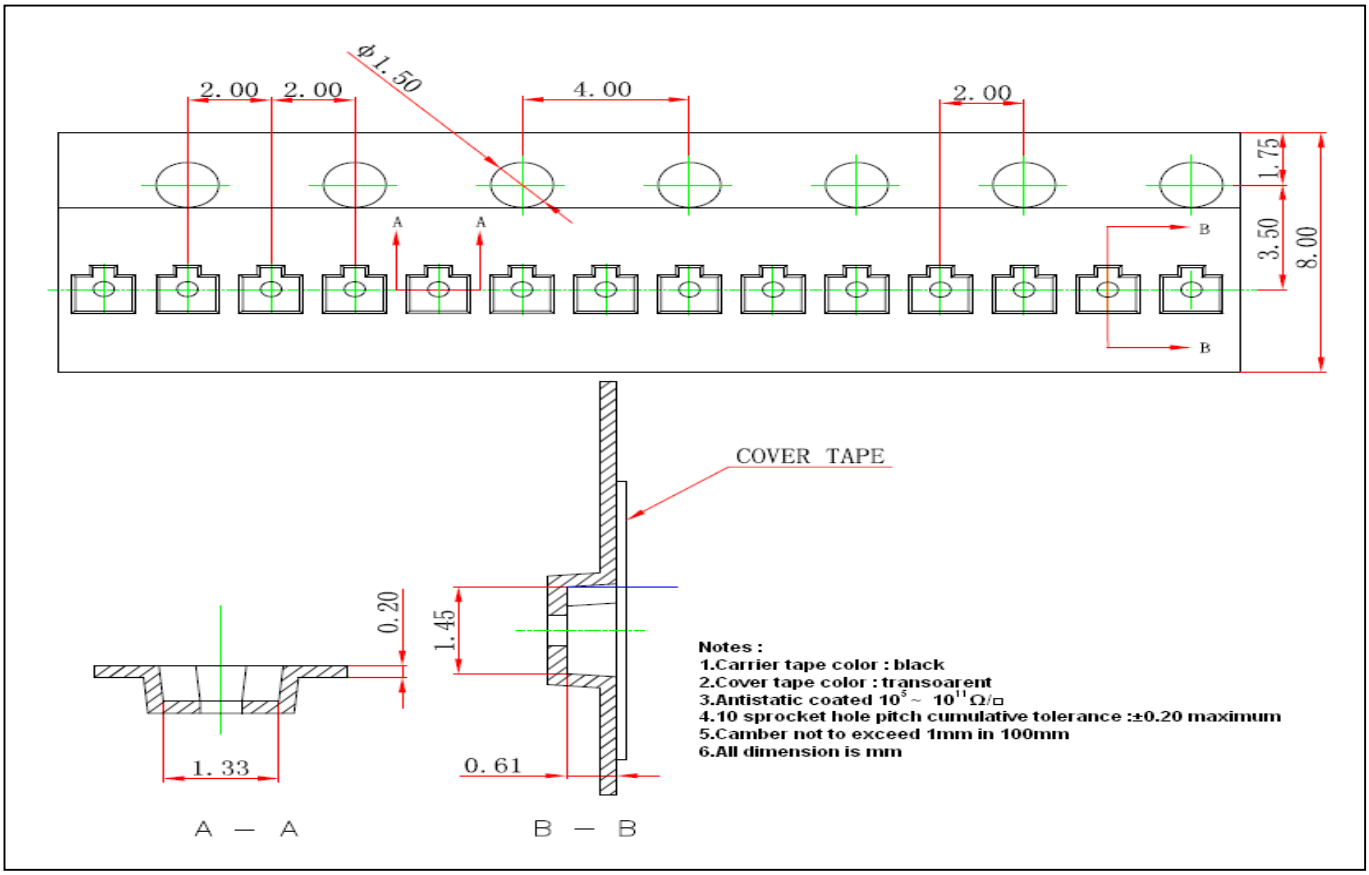
Power Derating Curve



Reel Dimension



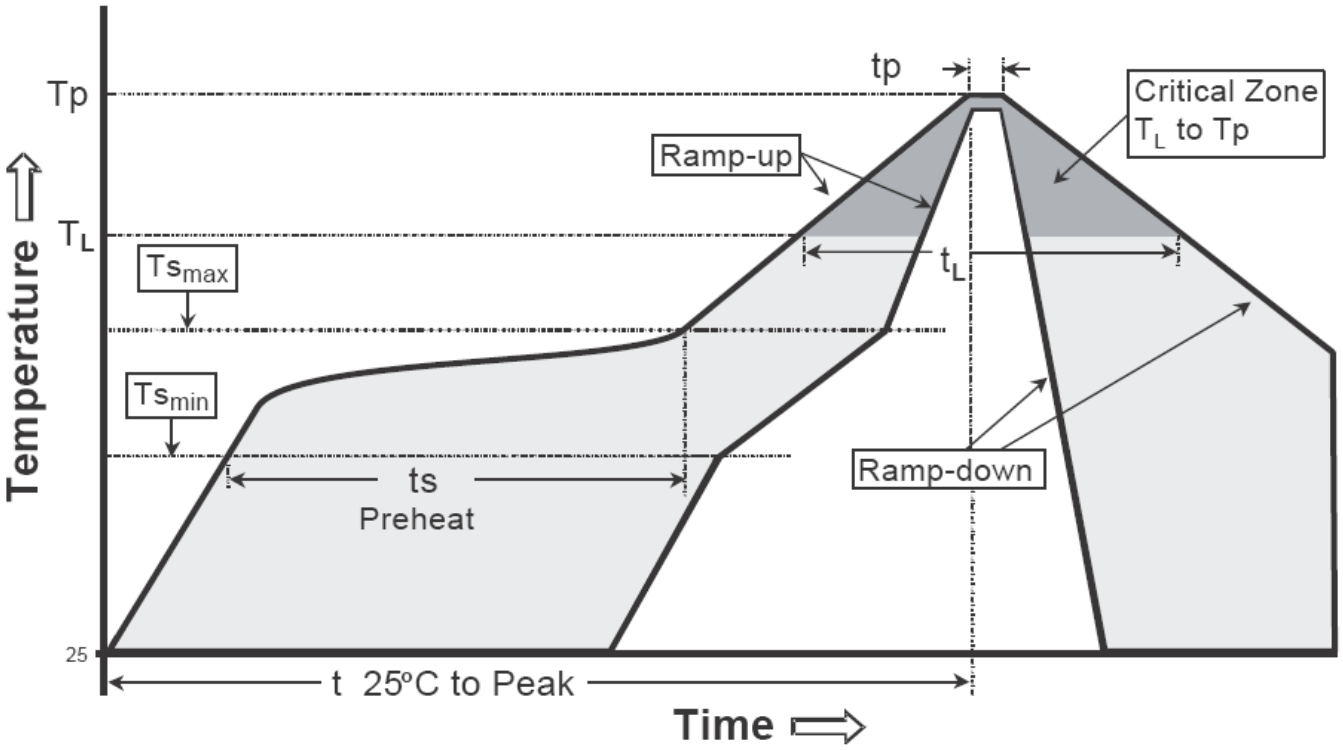
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

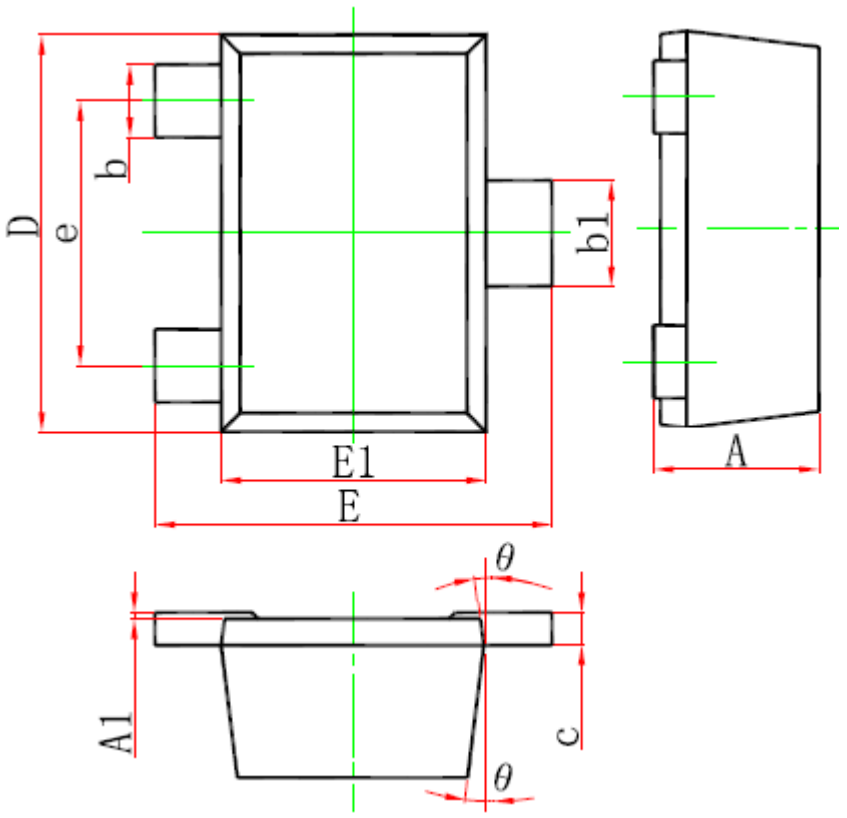
Recommended temperature profile for IR reflow

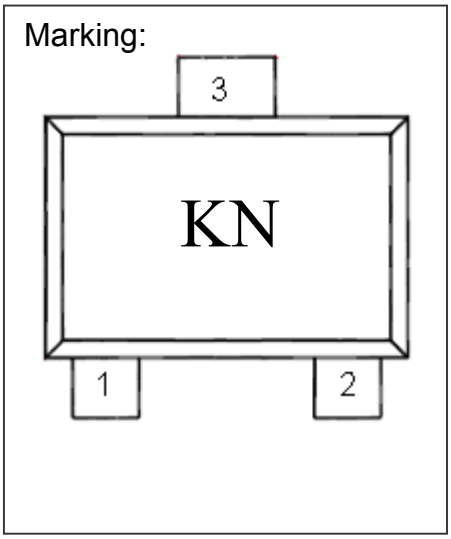


Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat −Temperature Min(T_S min) −Temperature Max(T_S max) −Time($t_{s\ min}$ to $t_{s\ max}$)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-180 seconds
Time maintained above: −Temperature (T_L) − Time (t_L)	 183°C 60-150 seconds	 217°C 60-150 seconds
Peak Temperature(T_P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note :1. All temperatures refer to topside of the package, measured on the package body surface.
2.For devices mounted on FR-4 PCB of 1.6mm or equivalent grade PCB. If other grade PCB is used, care should be taken to match the coefficients of thermal expansion between components and PCB. If they are not matched well, the solder joints may crack or the bodies of the parts may crack or shatter as the assembly cools.

SOT-723 Dimension





3-Lead SOT-723 Plastic
Surface Mounted Package
CYStek Package Code: Y3

Style: Pin 1.Gate 2.Source 3.Drain

*Typical

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.000	0.500	0.000	0.020	D	1.150	1.250	0.045	0.049
A1	0.000	0.050	0.000	0.002	E	1.150	1.250	0.045	0.049
b	0.170	0.270	0.007	0.011	E1	0.750	0.850	0.030	0.033
b1	0.270	0.370	0.011	0.015	e	0.800*		0.031*	
c	0.000	0.150	0.000	0.006	θ	7° REF		7° REF	

Notes: 1.Controlling dimension: millimeters.
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.